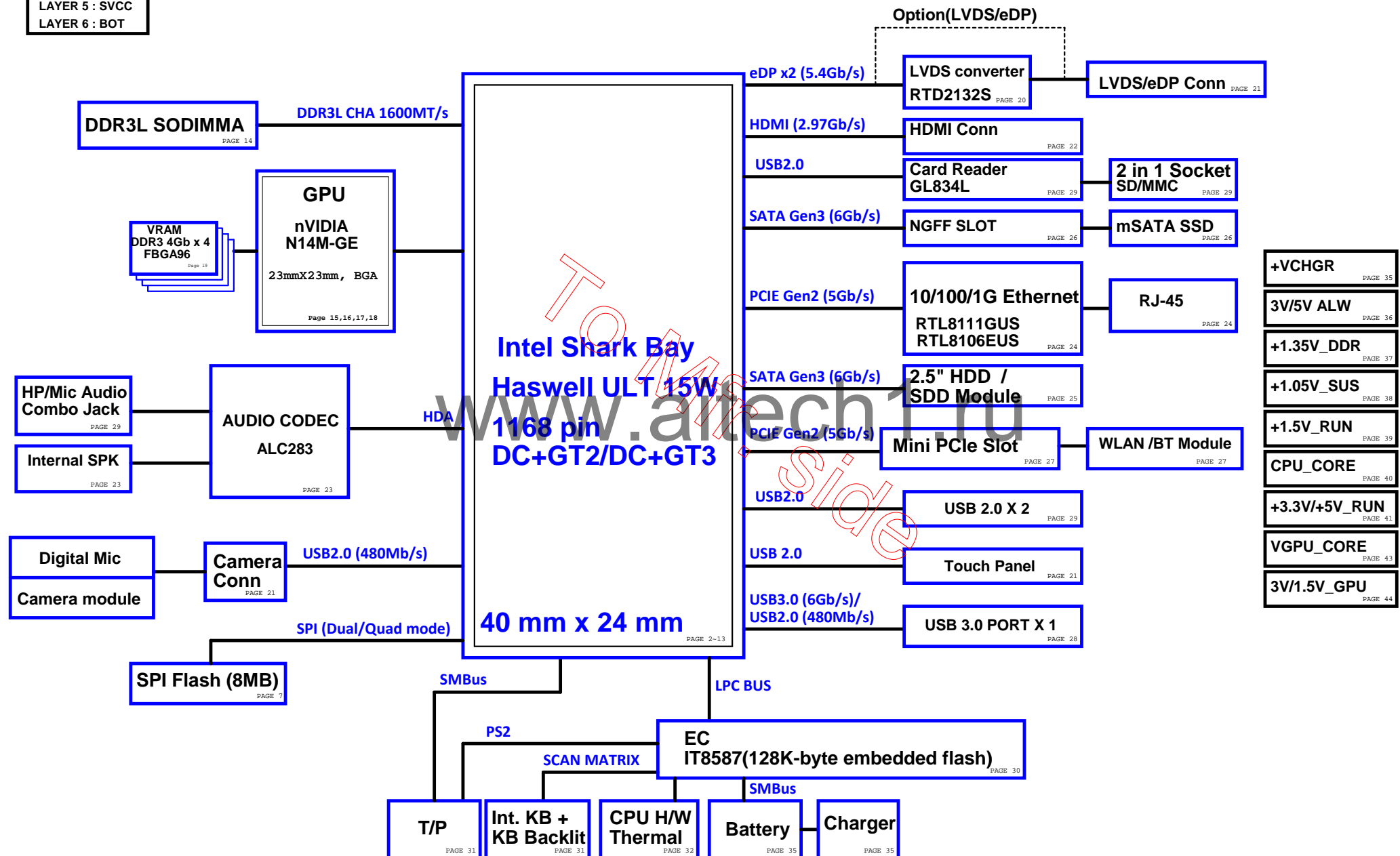


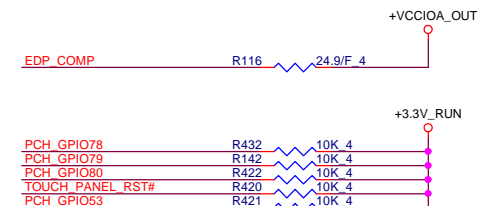
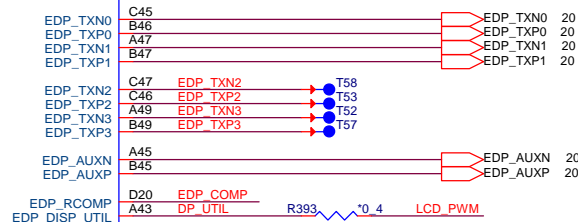
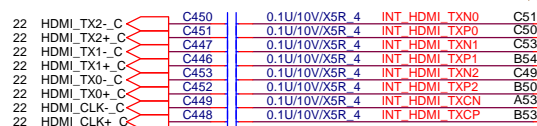
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

ST6/6A 14" OPTIMUS INTEL SHARK BAY ULT ONE CHIP PLATFORM

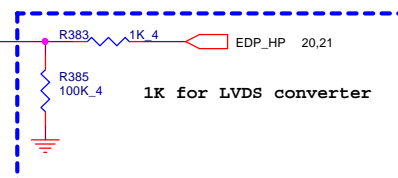
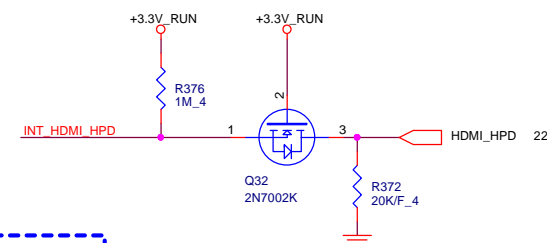
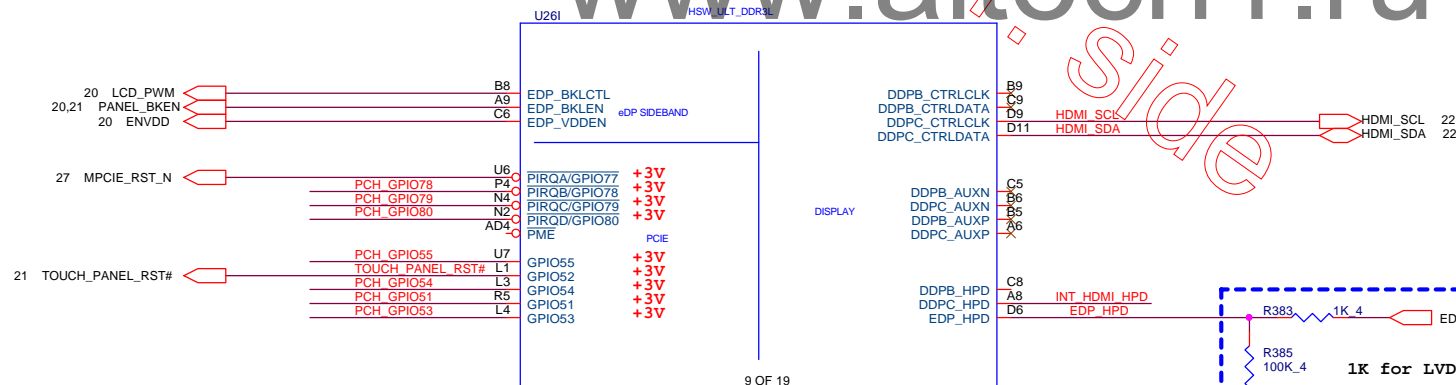
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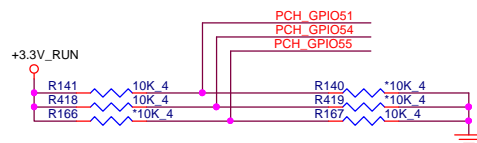
U26A		HSW_UL_T_DDR3L	
DDI1_TXN0			EDP_TXN0
DDI1_TXP0			EDP_TXP0
DDI1_TXN1			EDP_TXN1
DDI1_TXP1			EDP_TXP1
DDI1_TXN2			
DDI1_TXP2			EDP_TXN2
DDI1_TXN3			EDP_TXP2
DDI1_TXP3			EDP_TXN3
	DDI	EDP	EDP_TXP3
DDI2_TXN0			
DDI2_TXP0			EDP_AUXN
DDI2_TXN1			EDP_AUXP
DDI2_TXP1			
DDI2_TXN2			EDP_RCOMP
DDI2_TXP2			EDP_DISP_UTIL
DDI2_TXN3			
DDI2_TXP3			



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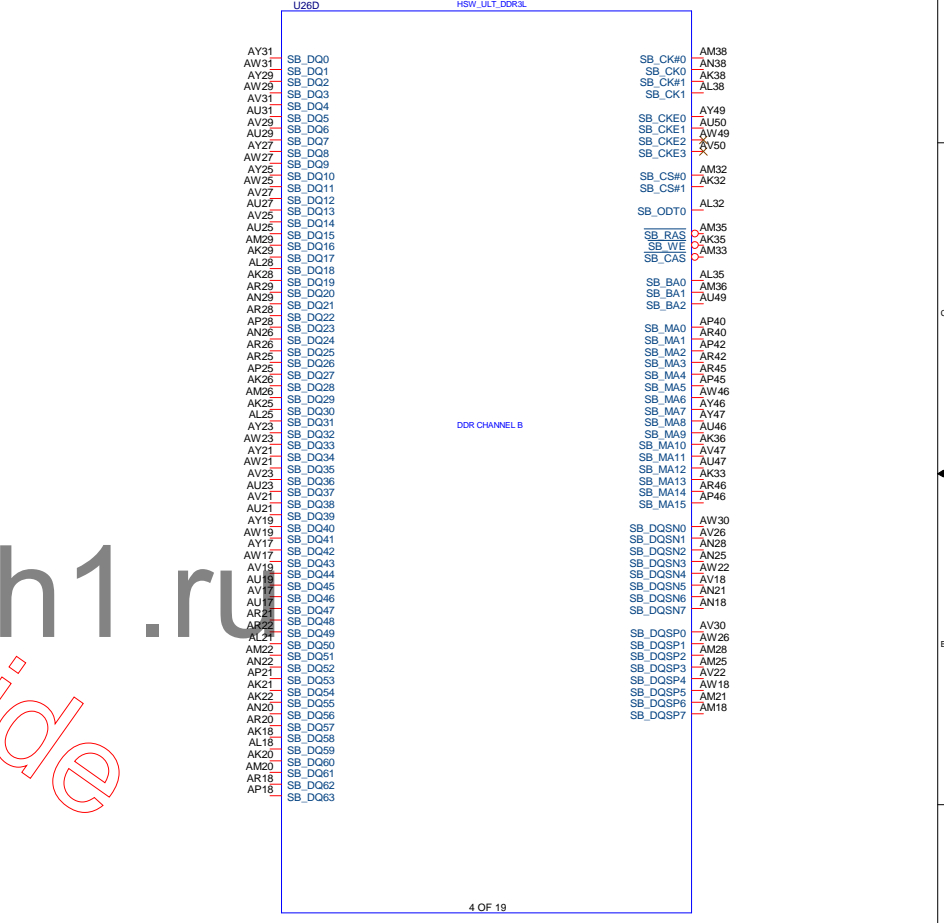
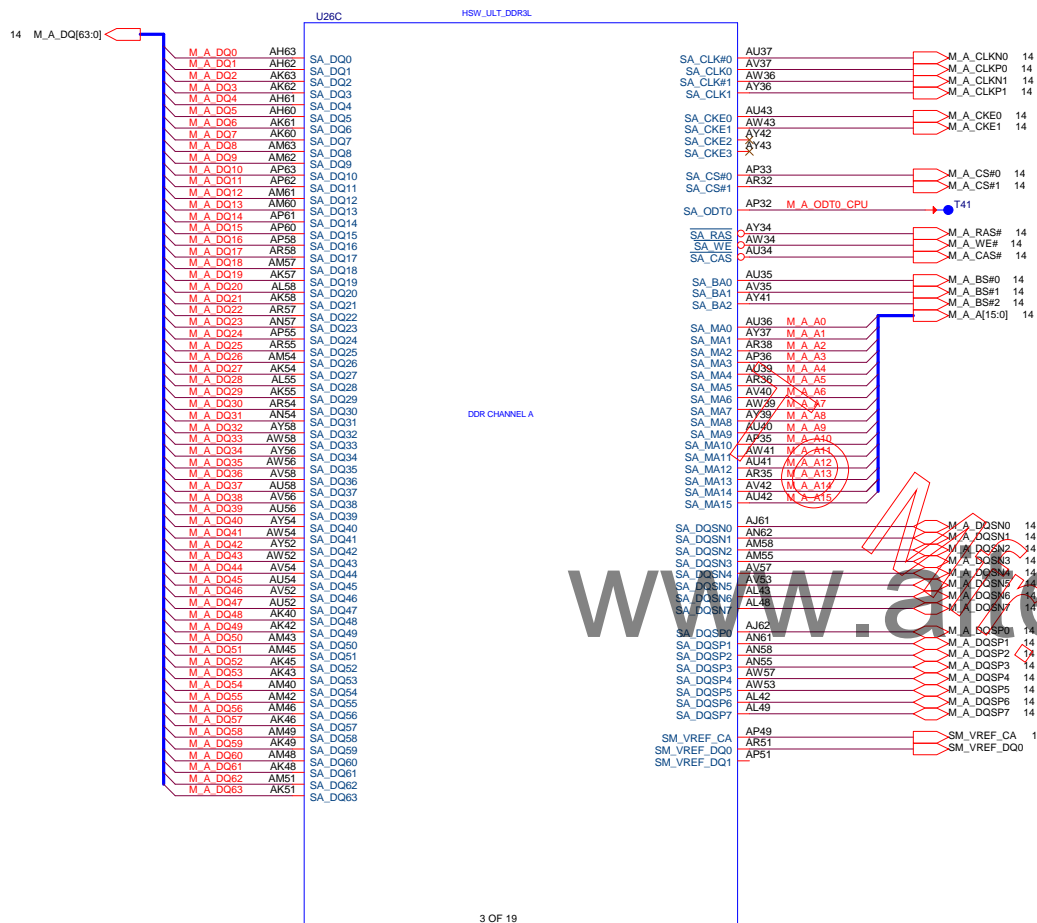


Board ID	GPIO51	GPIO54	GPIO55
SDV	1	1	1
SIV	1	1	0
SIT			
SVT			



Haswell ULT (DDR3L)

3



GPIO27

With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DsX

Haswell ULT(GPIO,LPIO,MISC)

+V1.05S_VCCST

R110 1K_4

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

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+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+3V

+V1.05S_VCCST 9,13
+3.3V_DEEP_SUS 5,6,7,8,12,14,34
+3.3V_RUN 2,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41,42
+3.3V_DSW 6,8,12,23,24,27,29,31,35,36,41,44

GPIO Pull-up/Pull-down(CLG)

SIO_WAKE_SCIN# R215 10K_4
GPIO12 R214 10K_4
GPIO25 R202 10K_4

GPIO26 R446 10K_4
SIO_EXT_SCIN# R445 10K_4
NGFF_SSD_PRESENT# R181 10K_4
WLAN_ON/OFF# R224 10K_4
GPIO28 R180 10K_4
BT_RADIO_DIS# R217 10K_4

GPIO76 R388 10K_4
GPIO90 R416 10K_4
TOUCH_PANEL_INTR# R433 10K_4
GPIO81 R108 10K_4
SIO_RCIN# R161 10K_4
GPIO88 R384 10K_4

VR TT# R386 10K_4
DEVSLP1 R417 10K_4
DEVSLP0 R434 10K_4
ALS_INT_N# R439 10K_4
GPIO17 R165 10K_4
TOUCH_FINGER_EN R145 10K_4
USB_ON R219 10K_4
USB3_P0_EN R469 10K_4
GFXPG R34 10K_4

DGPU_HOLD_RST# R390 10K_4
NGFF_WLAN_PWR_EN R139 10K_4
CCD_EN R438 10K_4
PCH_OPIRCOMP R478 49.9F_4
ADP_TYPE_0 R190 10K_4
ADP_TYPE_1 R174 10K_4

GPIO92 R415 10K_4

GPIO91 RN4 1 2 10K
SDA_ALS_L 3 4
SCL_ALS_L 5 6
GPIO94 7 8
GPIO88 R389 10K_4

GPIO1 RN21 2 10K
GPIO3 3 4
GPIO2 5 6
GPIO0 7 8

GPIO67 RN11 2 10K
GPIO65 3 4
GPIO64 5 6
GPIO69 7 8

CLK_RTD R399 10K_4
DAT_RTD R398 10K_4

GPIO56 10K_4 R196
GPIO57 10K_4 R466
GPIO58 10K_4 R220
GPIO59 10K_4 R227
GPIO46 10K_4 R200

DGPU SELECT	GPIO39
UMA	1
DIS	0

Model ID	GPIO45
S14	0
S15	1

VRAM Freq.	GPIO68
1G	1
900M	0

+3.3V_RUN R144 10K_4 GPIO39 R143 DIS@10K_4

+3.3V_DEEP_SUS R464 10K_4 GPIO45 R460 10K_4

+3.3V_RUN R387 10K_4 GPIO68 R401 DIS@10K_4

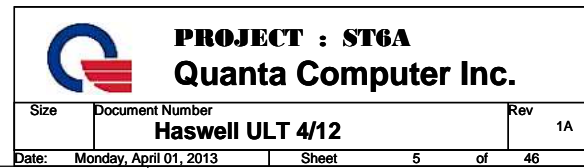
HW board ID to distinguish VRAM 900MHz & 1GHz

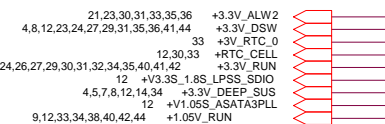
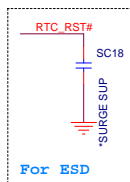
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Quanta Computer Inc.

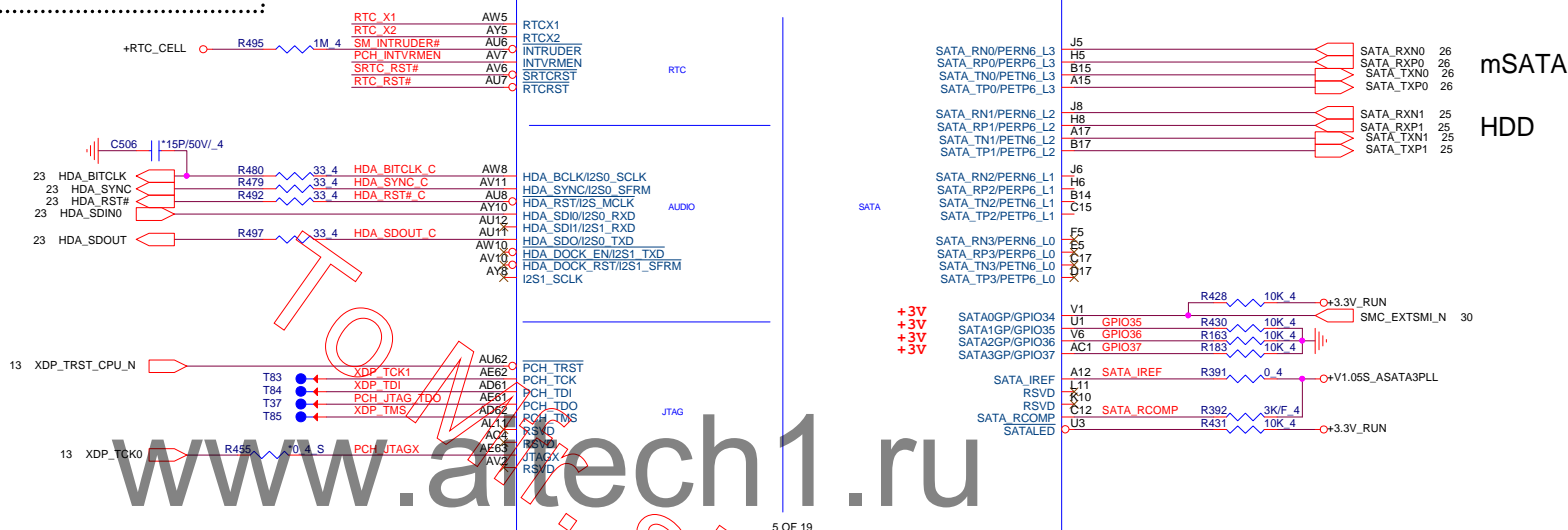
Size	Document Number	Rev
	Haswell ULT 3/12	1A
Date:	Monday, April 01, 2013	Sheet 4 of 46








U26K HSW_ULT_DDR3L

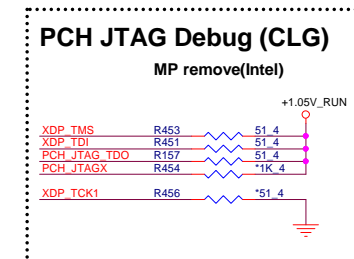





6



Pin Name	Strap description	Sampled	Configuration	Note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_RUN 
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	30 ME_WR# 
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL 
GPIO66	Top-Block Swap override		0 = Default disable (iPD 20K) 1 = Enable TBS function	+V3.3S_1.8S_LPSS_SDIO 
GPIO86	BBS(Boot BIOS Strap Bit)		0 = Default SPI (iPD 20K) 1 =LPC	+3.3V_RUN 
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality(iPD 20K) 1 =Default enable with confidentiality	+3.3V_DEEP_SUS 
DSWVREN	Deep Sx well on die DSW VR enable		1=Should be always pull-up	+RTC_CELL 

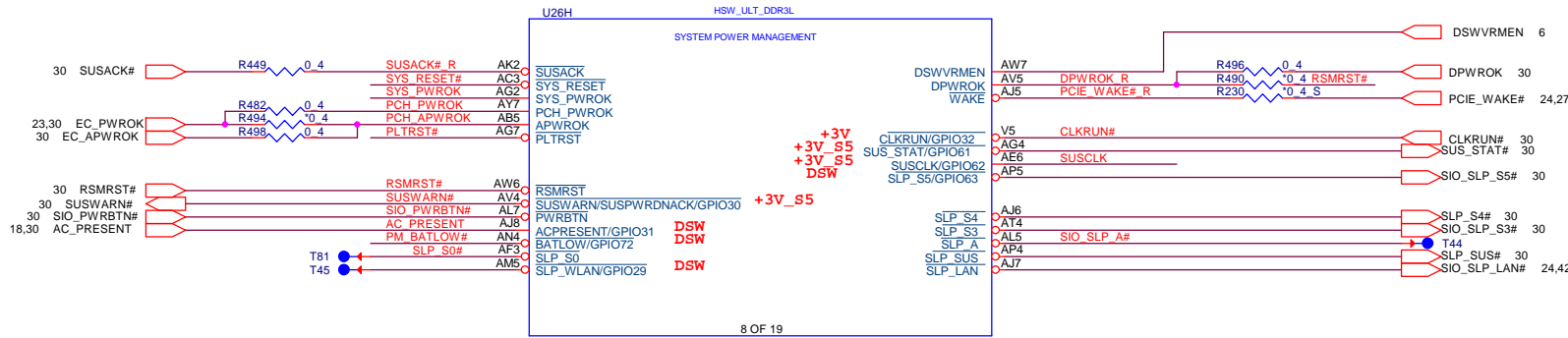


	PROJECT : ST6A Quanta Computer Inc.		
	Size	Document Number Haswell ULT 5/12	Rev 1A
Date: Monday, April 01, 2013	Sheet	6 of 46	

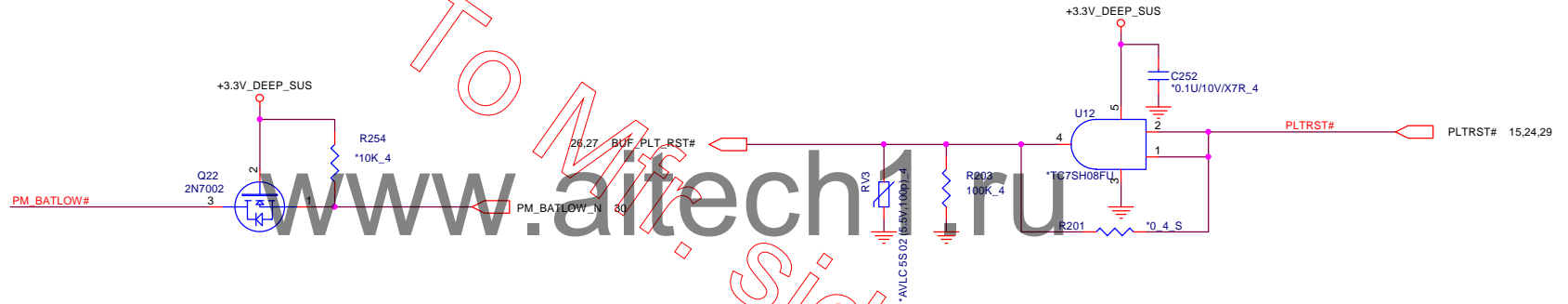
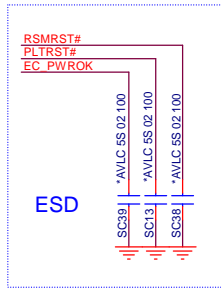
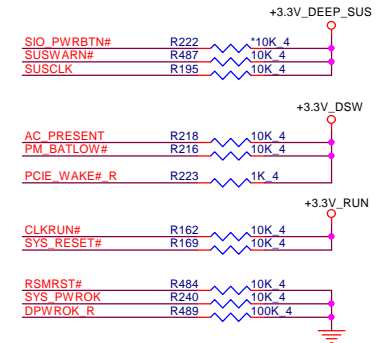
Haswell ULT (SYSTEM POWER MANAGEMENT)

4,6,12,23,24,27,29,31,35,36,41,44 +3.3V_DSW
2,4,6,7,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41,42 +3.3V_RUN
4,5,6,7,12,14,34 +3.3V_DEEP_SUS

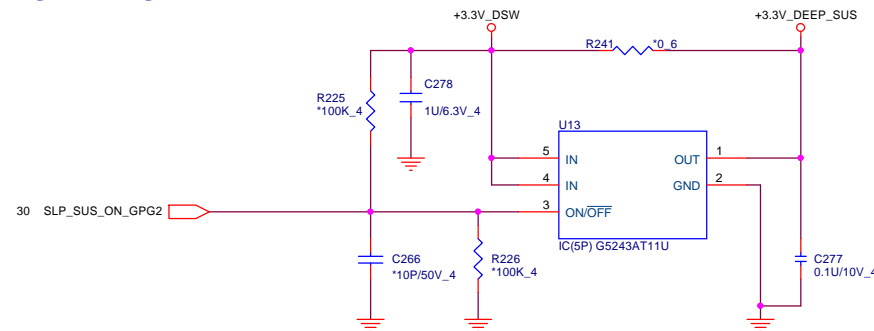
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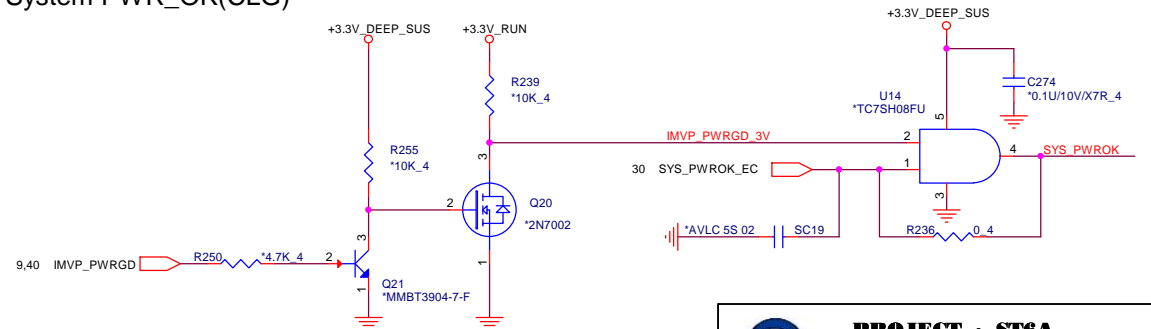
PCH Pull-high/low(CLG)



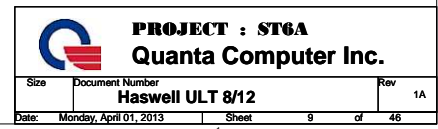
For DS3

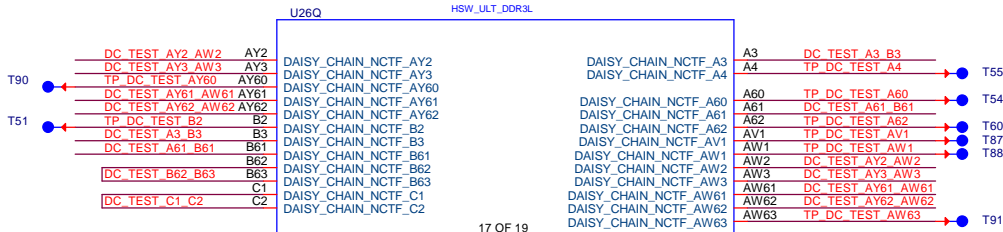
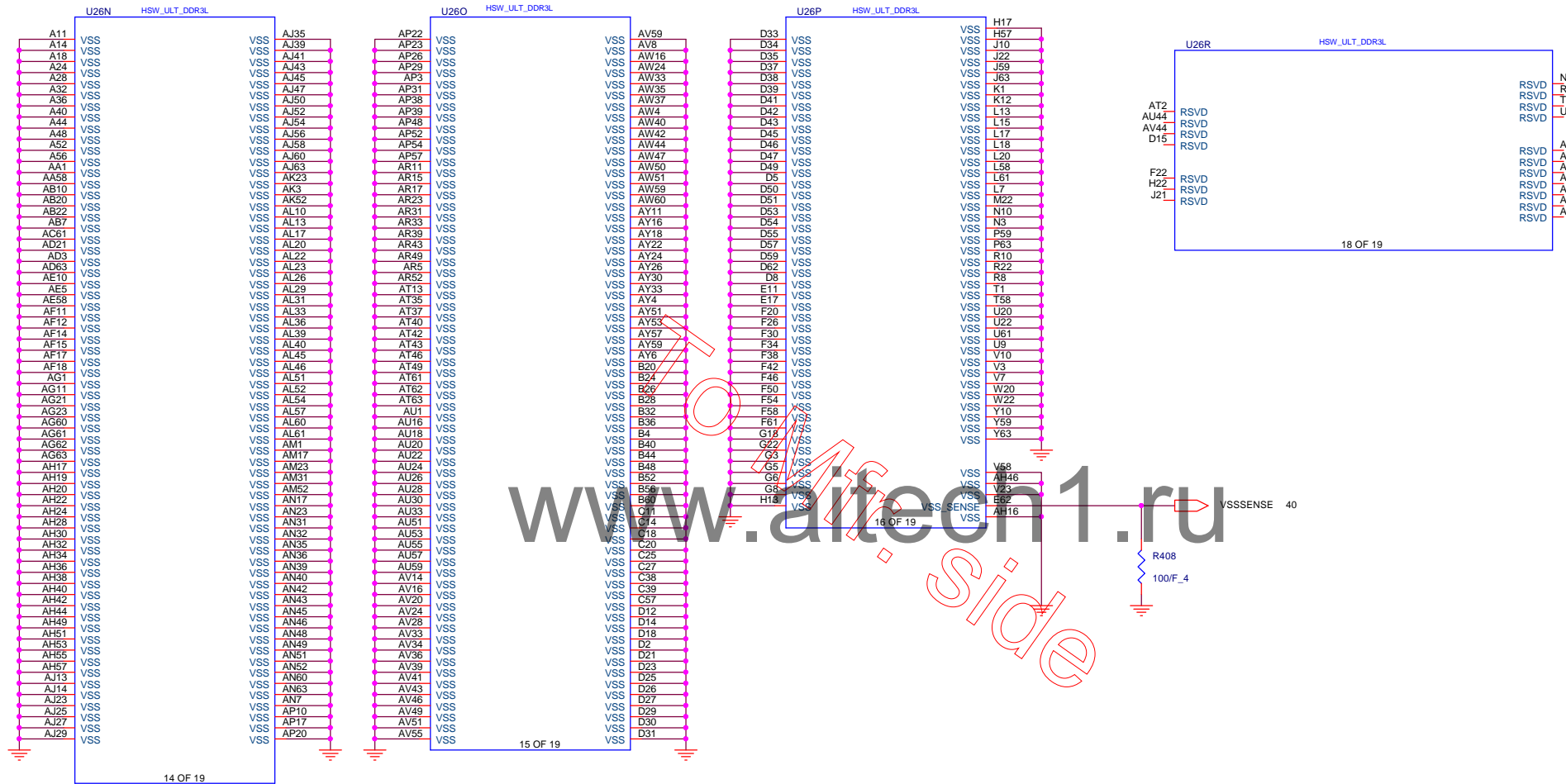


System PWR_OK(CLG)



Haswell ULT 15W : 32A

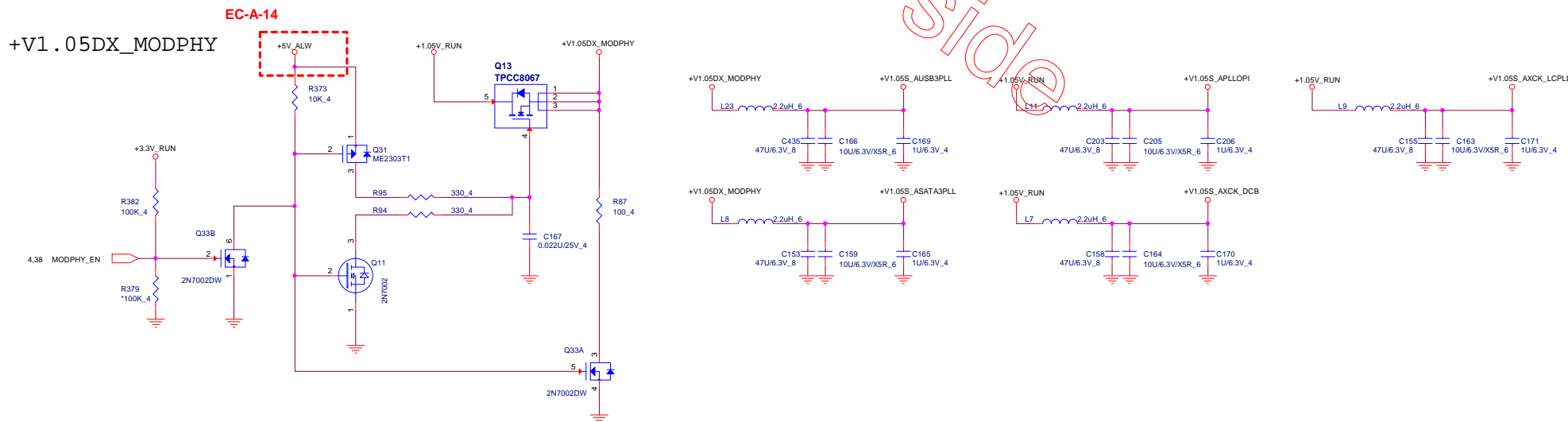
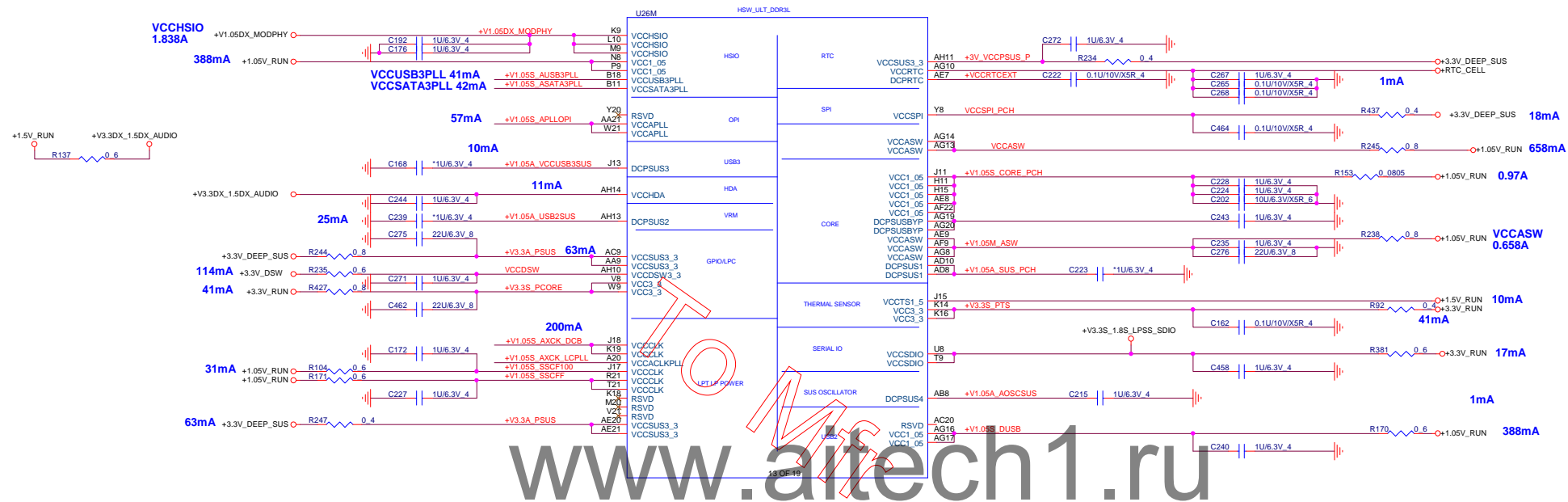


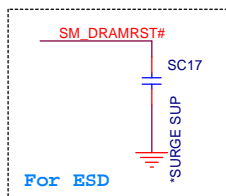


Haswell ULT PCH(POWER)

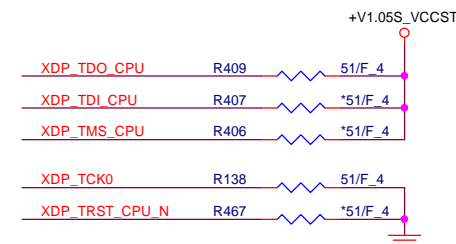
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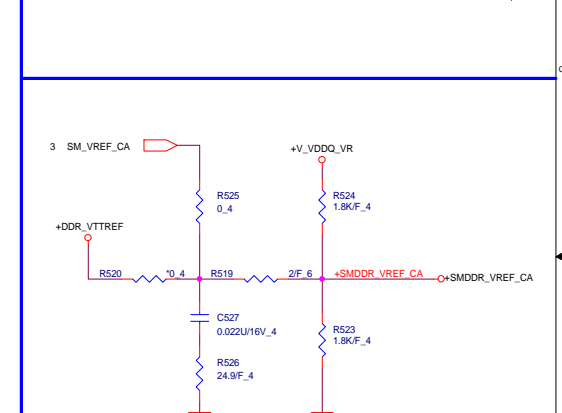
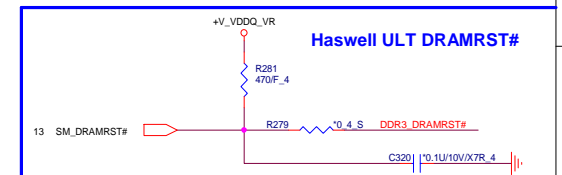
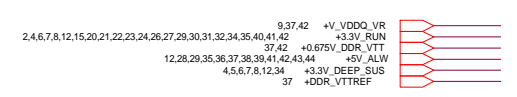
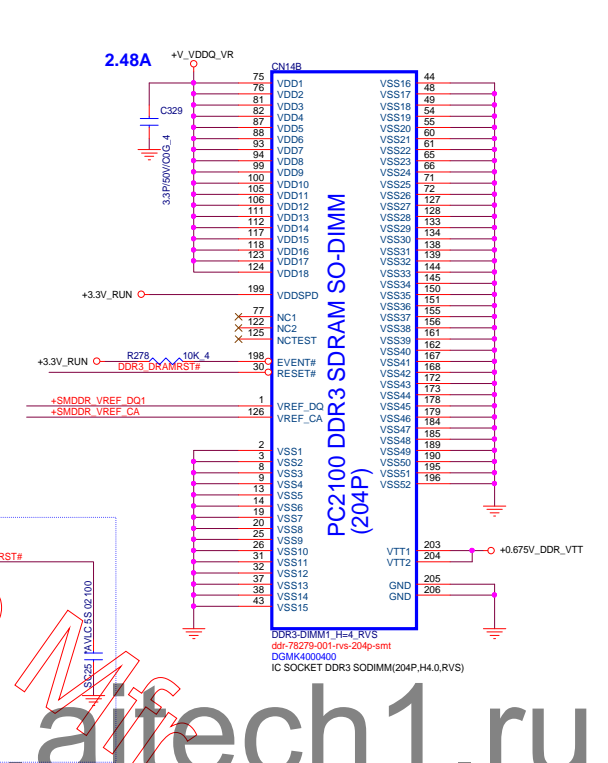
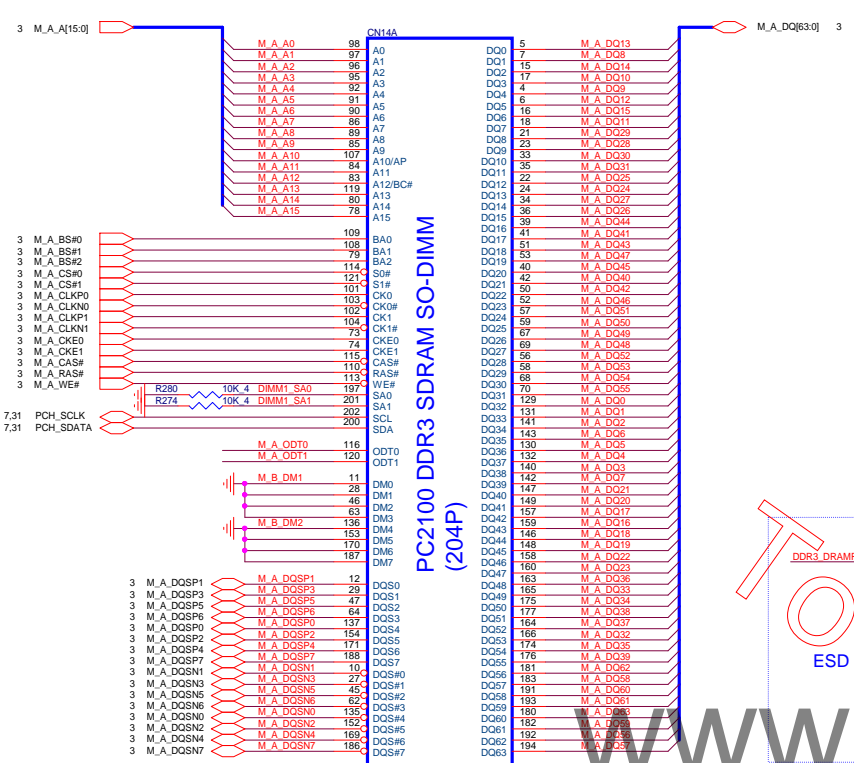
6,9,33,34,38,40,42,44 +1.05V_RUN
4,5,6,7,8,14,34 +3.3V_DEEP_SUS
4,6,8,23,24,27,29,31,35,36,41,44 +3.3V_DSX
2,4,6,7,8,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41,42 +3.3V_RUN
23,27,34,39,42,44 +1.5V_RUN
36,41,44 +1.5V_ALW
6,30,33 +RTC_CELL
5 +V1.05S_AUSB3PLL
6 +V1.05S_ASATA3PLL
7 +V1.05S_AXCK_LCPLL



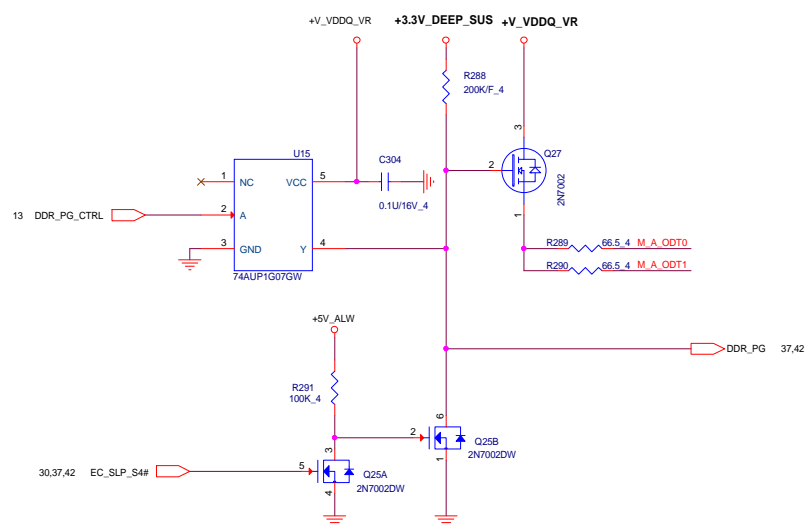


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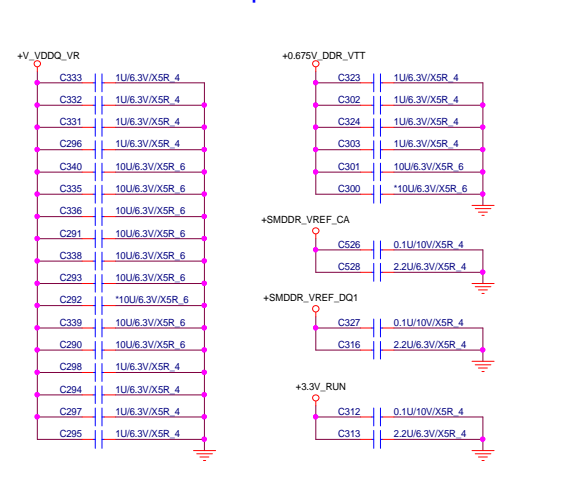




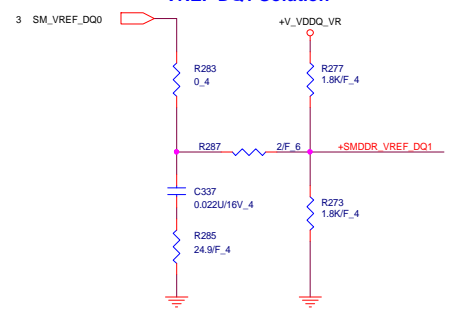
DDR3L SODIMM ODT DERATION



Place these Caps near So-Dimm1



VREF DQ1 Solution



Peak current:40.89A
Boosted:28A
EDP-C:35A

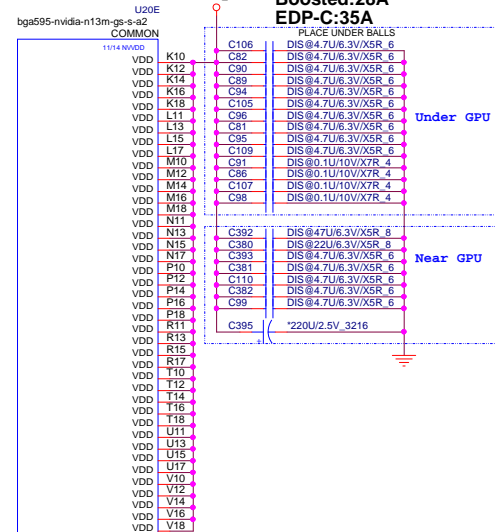


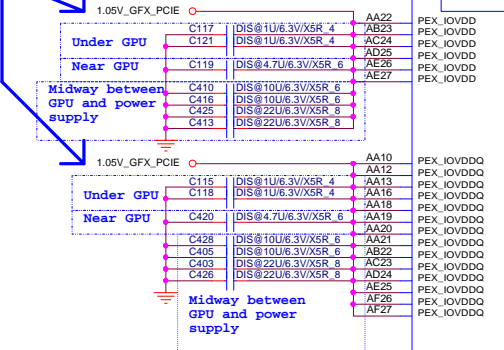
Table 2. GPU Power Rails

Notes: 1. The same power plane can be used for VDD33 and DAC_{IC}_VDD.
2. Voltage depends on memory type and SKU.
3. Voltage depends on the IFP link (see Chapter 8, Digital Displays)
4. On GB1-256, GB2-192 and some SKUs of GB4-128, the VDD33 rail is separated into VDD33 and 3V3MISC, where 3V3MISC is an isolated rail on the package and silicon. See section 18.7.12 in this document.

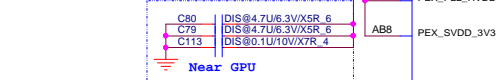
PROJECT : ST6A
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<VGA>

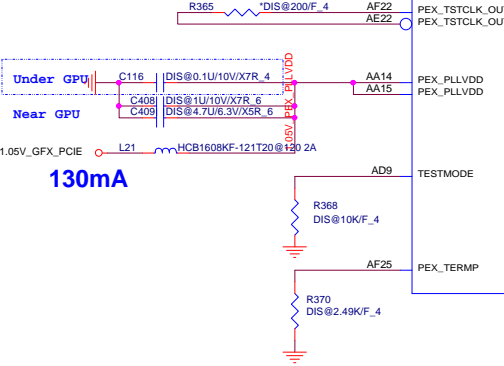
855mA



286mA

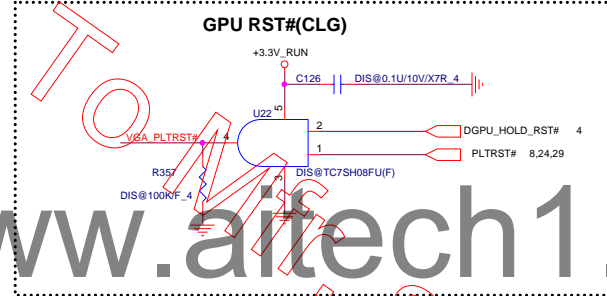


12~16 mils

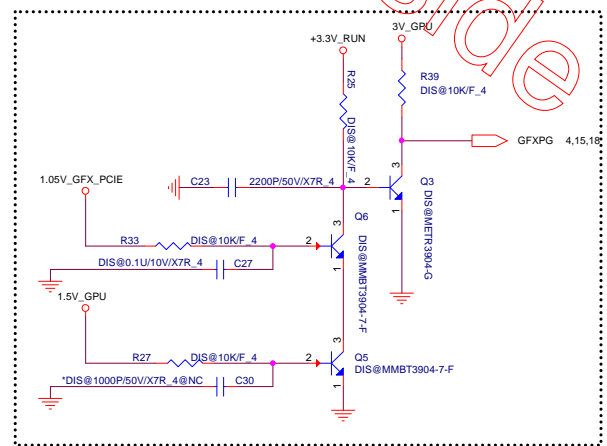


130mA

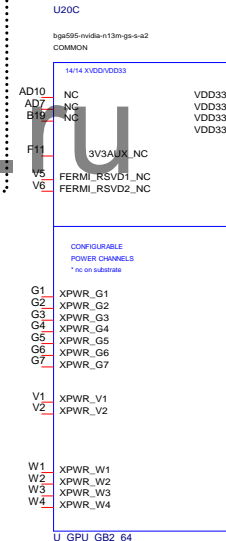
GPU RST#(CLG)



GPU RST#(CLG)



U20C
bga595-nvidia-n13m-gs-s-a2
COMMON



U_GPU_GB2_64

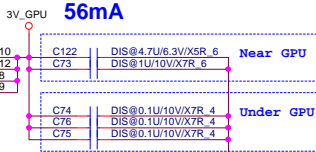
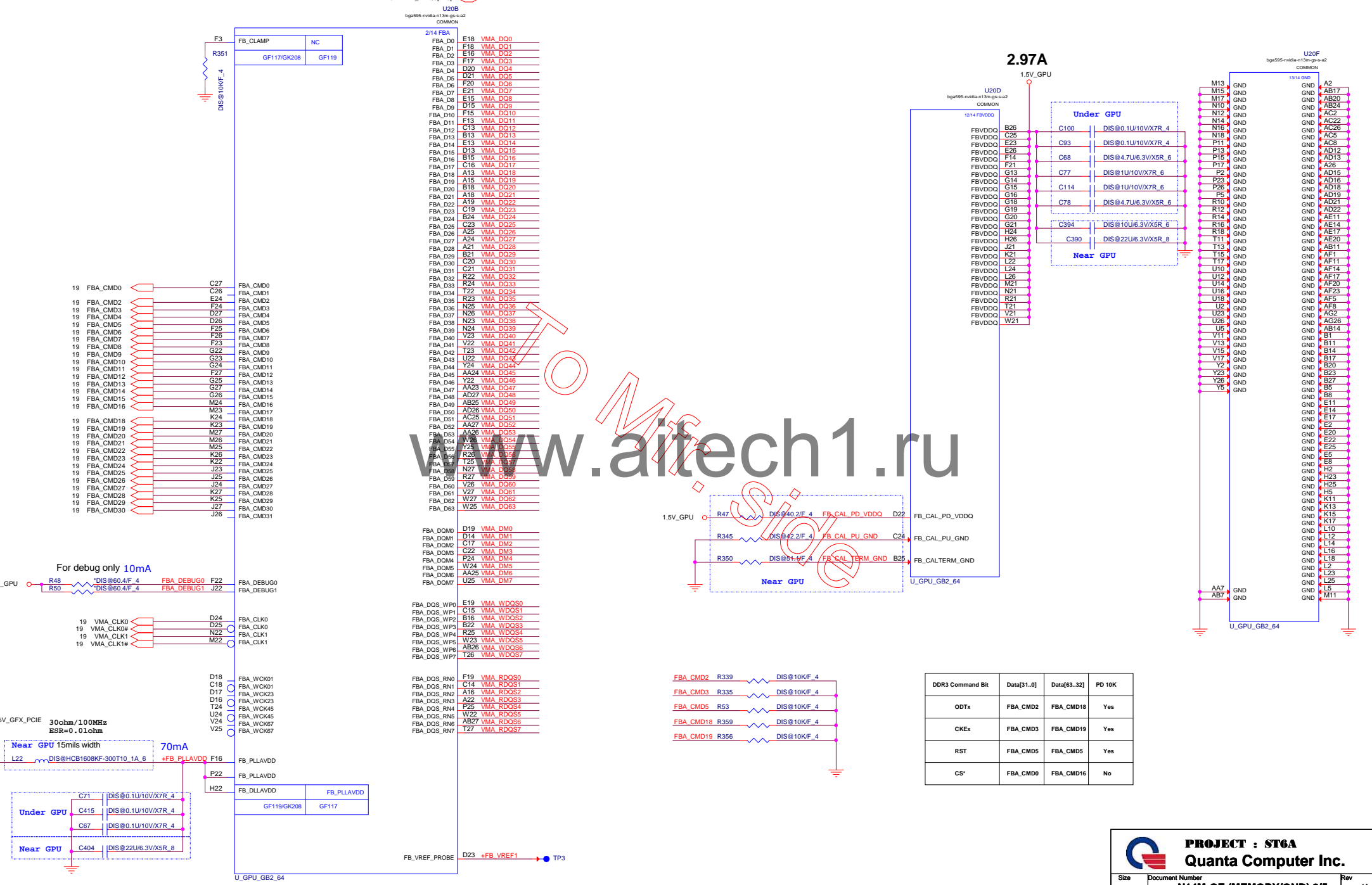


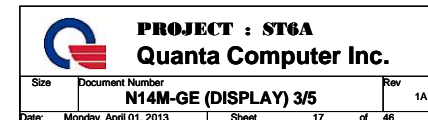
Table 2. GPU Power Rails

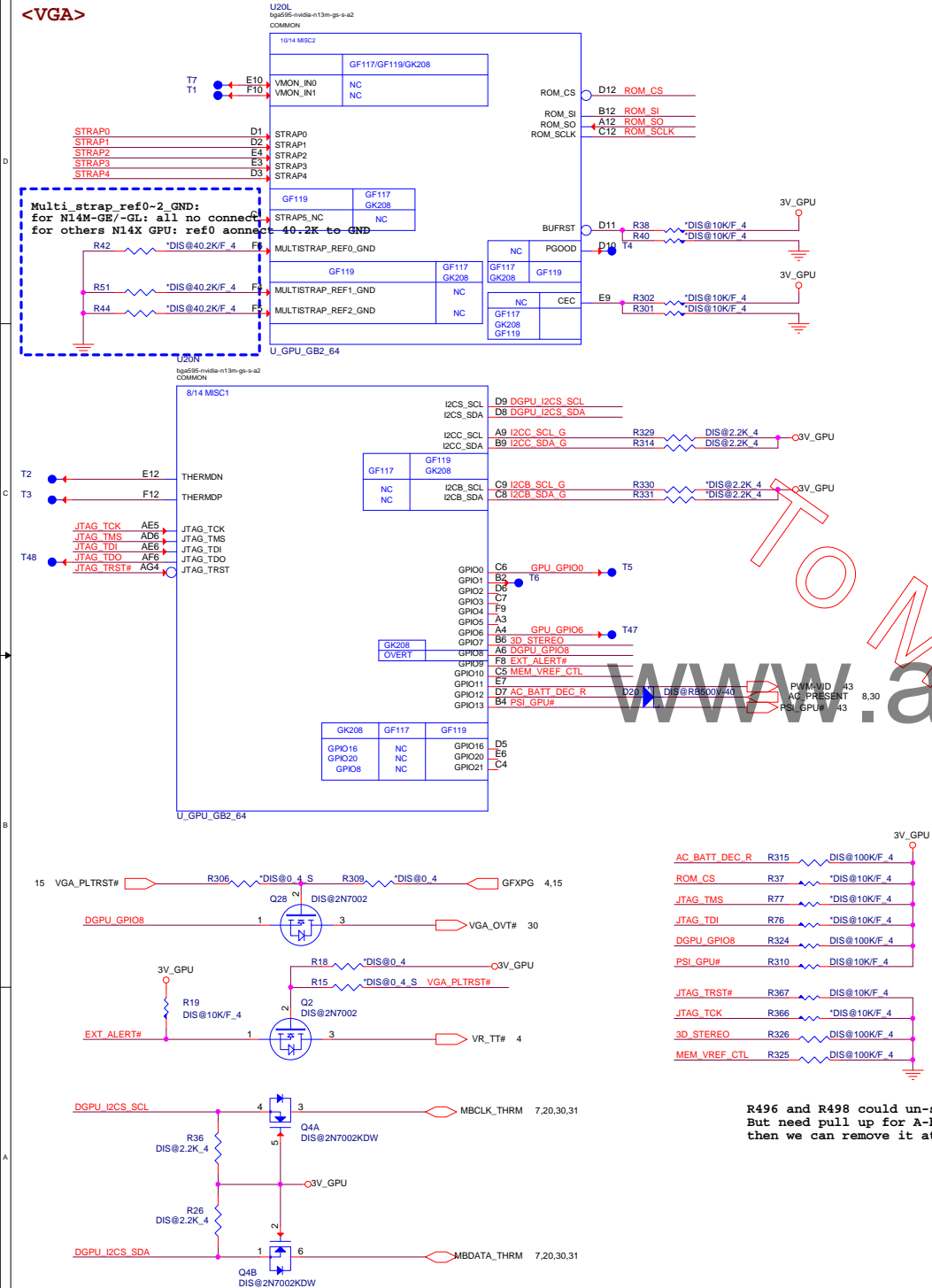
Notes: 1. The same power plane can be used for VDD33 and DAC_{IC}_VDD.
2. Voltage depends on memory type and SKU.
3. Voltage depends on the IFP link (see Chapter 8, Digital Displays)
4. On GB1-256, GB2-192 and some SKUs of GB4-128, the VDD33 rail is separated into VDD33 and 3V3MISC, where 3V3MISC is an isolated rail on the package and silicon. See section 18.7.12 in this document.

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Optimus:
All unstuff , one Cap stuff 10K ohm

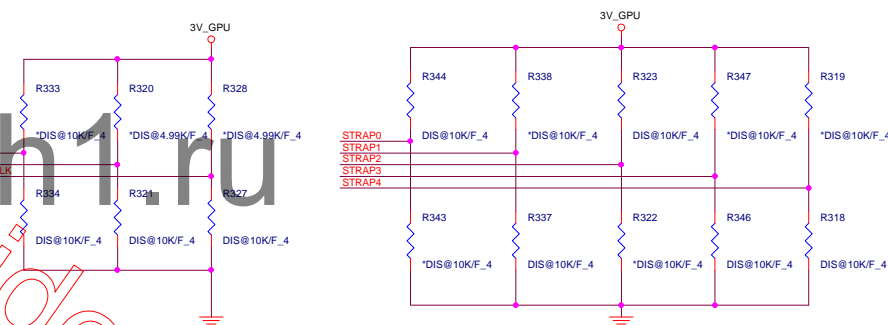




Res	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	XXXX
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVIDE[5]	PEX_PLL_EN_TERM	XXXX
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	0111

1GHz	Samsung	K4W2G1646E-BC1A	AKD5MGGT532
	Micron	MT41J128M16JT-093G:K	AKD5MGSTL15
	Hynix	Hynix 128x16 Vram H5TC2G63FFR-11C	AKD5MZDTW04
900MHz	Samsung	K4W4G1646B-HC11	AKD5MGWT516
	Micron	MT41K256M16HA-107G:E	AKD5PGSTL00



GPIF150		N14M-GE-A3
Item		
Device ID		051110
Package		084-128/082-64
Internal P/N		GF117_28nm
ROM_S1		10kohm pull down
ROM_S0		10kohm pull down
ROM_SCLK		10kohm pull down
Strap0		
Strap1		
Strap2		
Strap3		
Strap4		
Open_VREG_SKU		10kohm pull down
CoreFG		0.9V
NVVD0 Boot Voltage		0.9V

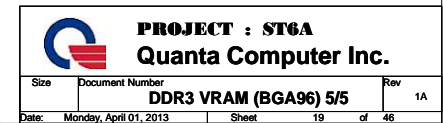
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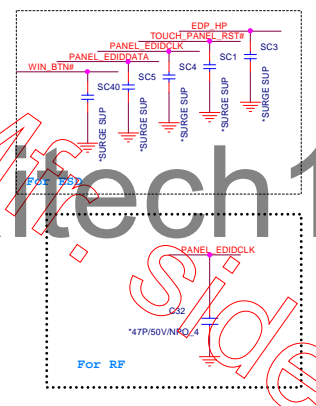
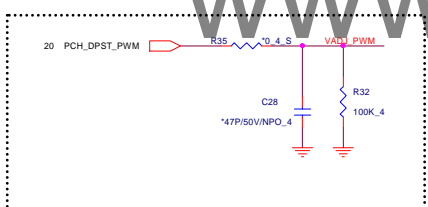
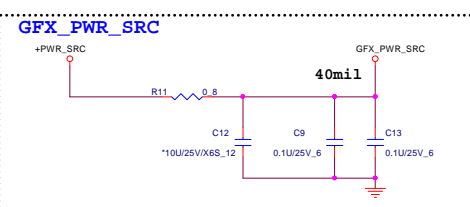
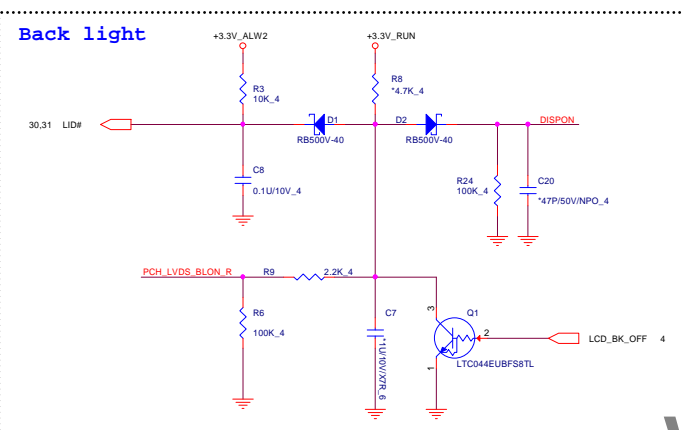
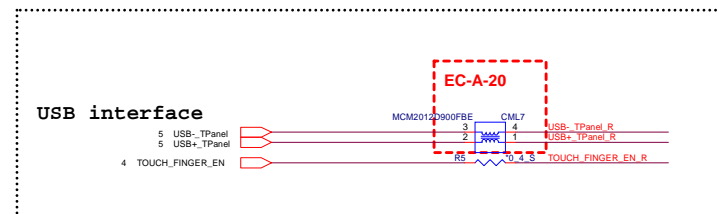
R496 and R498 could un-stuff for cost saving. But need pull up for A-build, if no problem then we can remove it at next build.



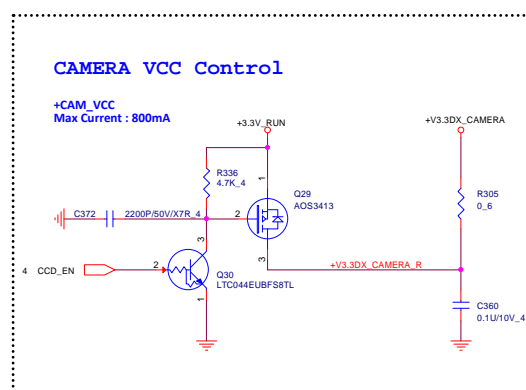
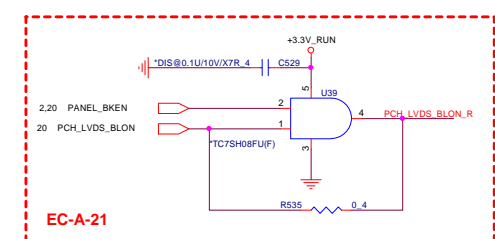
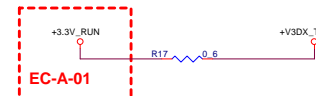
PROJECT : ST6A
Quanta Computer Inc.

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	N14M-GE (GPIO/STRAPS) 4/5	1A
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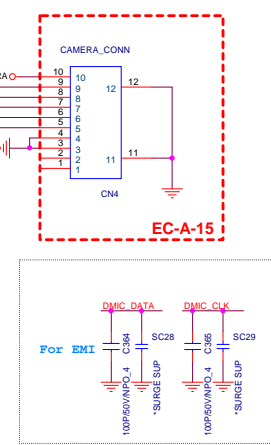
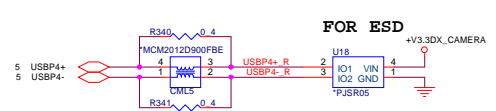
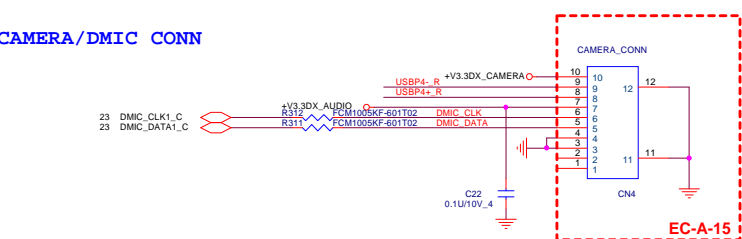


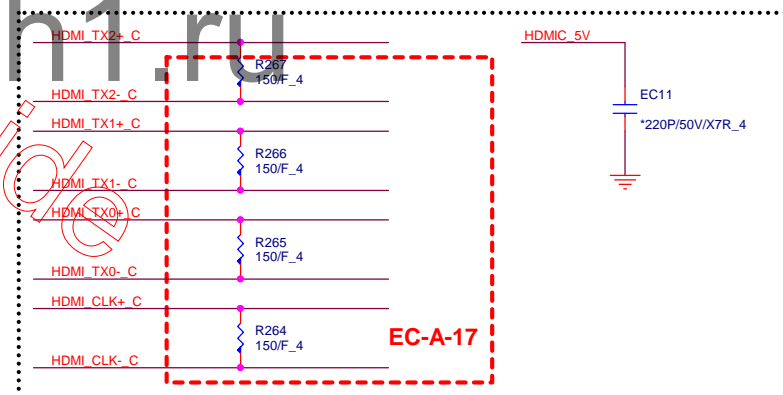


Touch Panel VCC Control

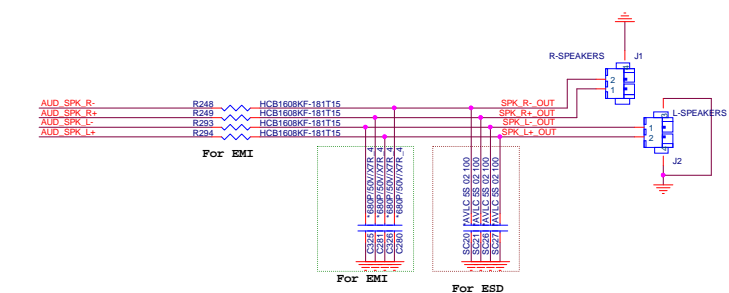
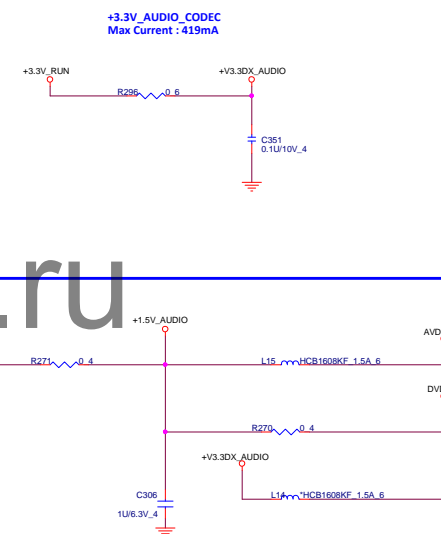
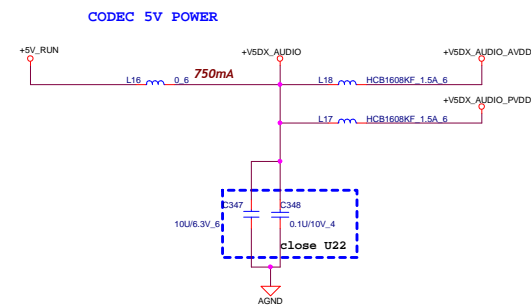
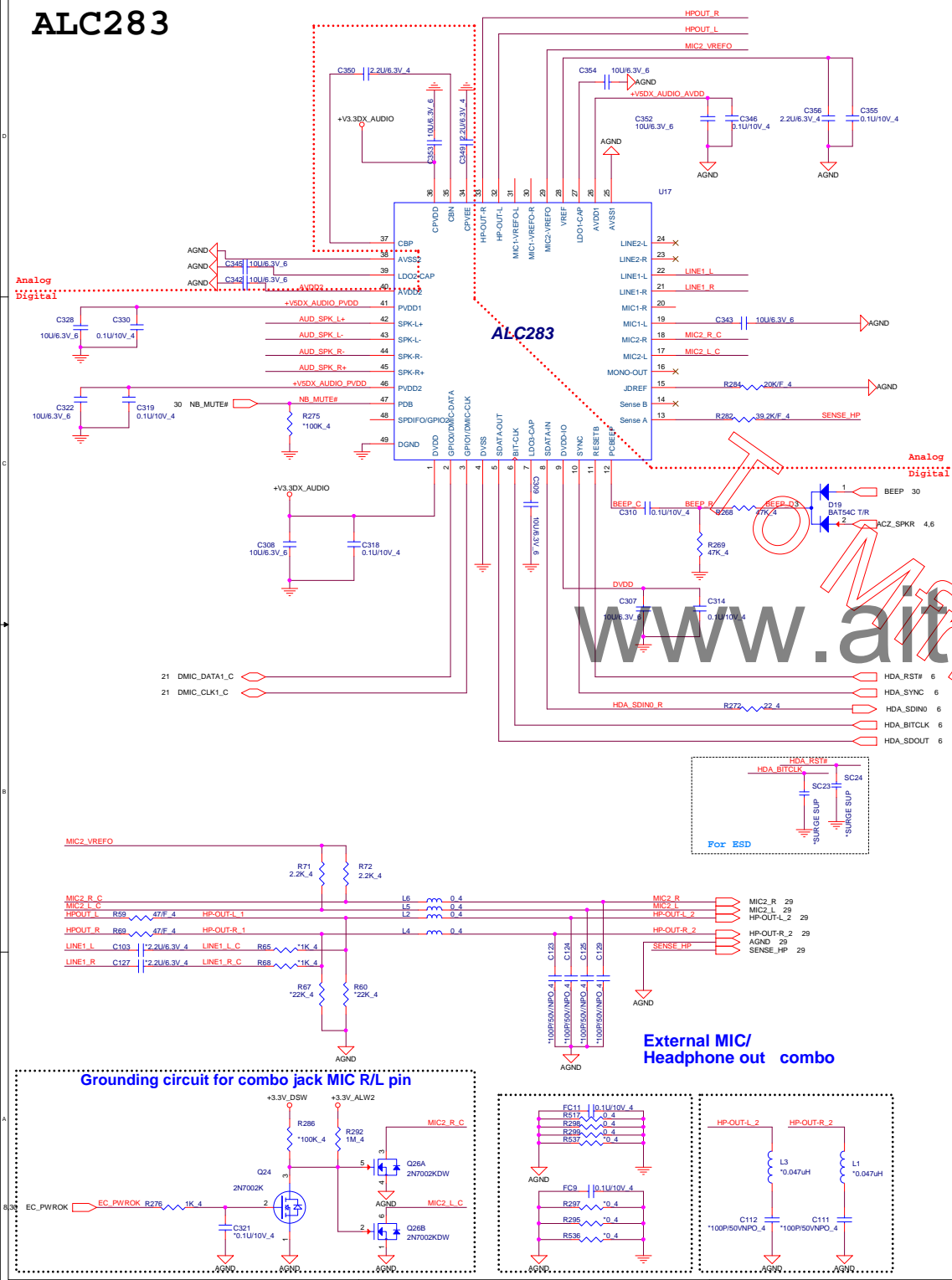


CAMERA/DMIC CONN

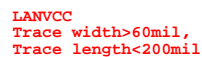




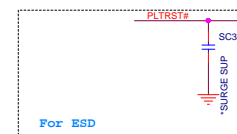
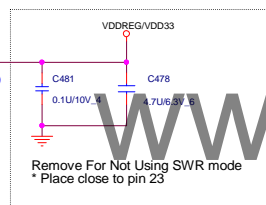
ALC283



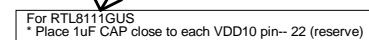
INT Speaker



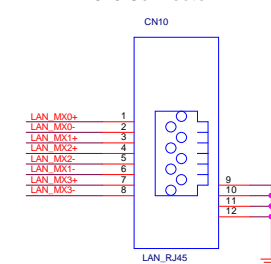
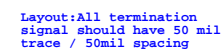
10/100	RTL8106EUS-CG	AL008106002
1G	RTL8111GUS-CG	AL008111009

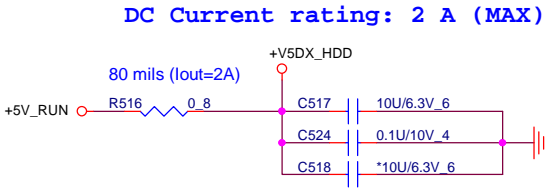
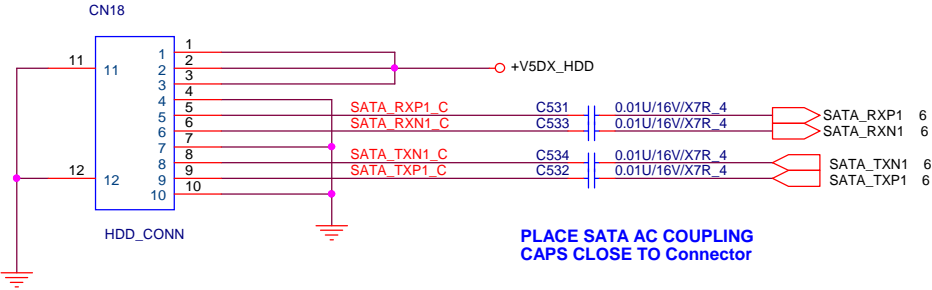


For RTL8111GUS
* Place 0.1uF CAP close to each
VDD10 pin-- 3, 8, 22, 30 For RTL8106E
* Place 0.1uF CAP close to each VDD10 pin-- 8, 30
40 mils (out=1A)



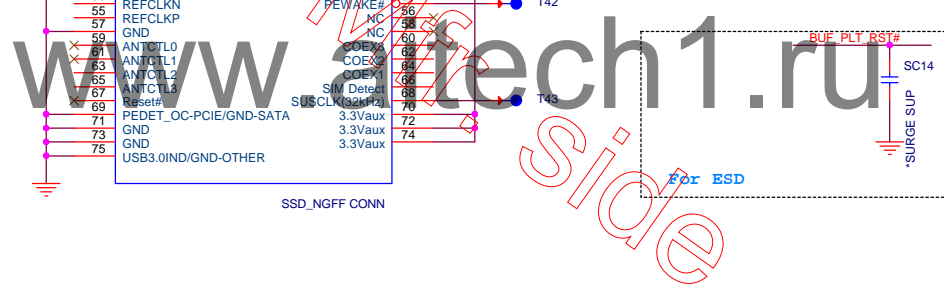
The image contains two circuit diagrams. The left diagram shows the LDO mode for the RTL8111G, featuring a VDDREG/VDD33 pin connected to a 4.7uF/6.3V capacitor (C478) and a 0V pin. The right diagram shows the LDO mode for the RTL8111GUS, featuring a REGOUT pin connected to a 40mA load (IOUT=1A) and a 4.7uH inductor (L13), followed by a 4.7uF/6.3V capacitor (C251) and a 0V pin. A large red watermark 'www.aitech1.com' is overlaid across the center, and a red 'Slide' watermark is in the bottom right corner.





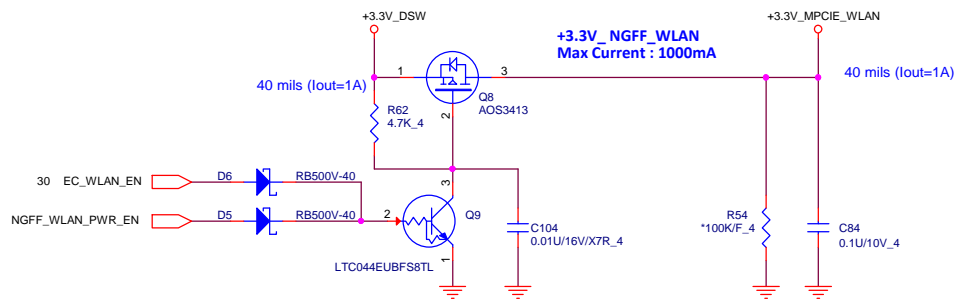
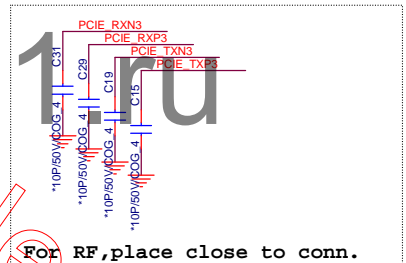
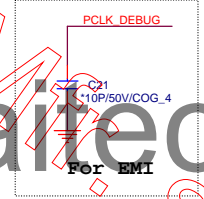
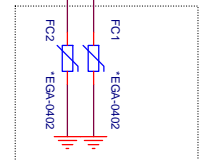
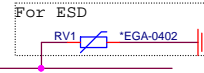
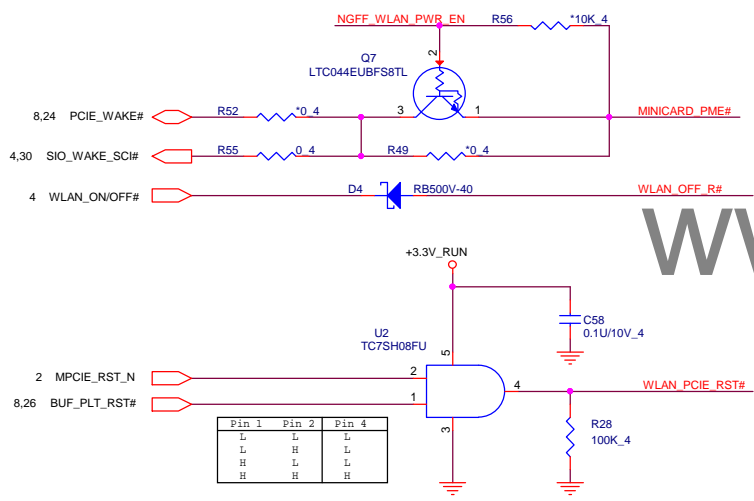
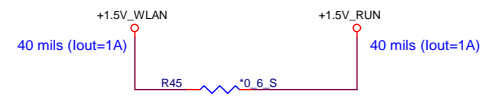
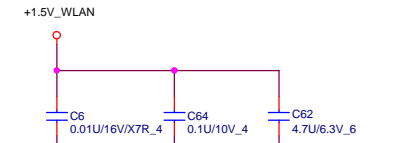
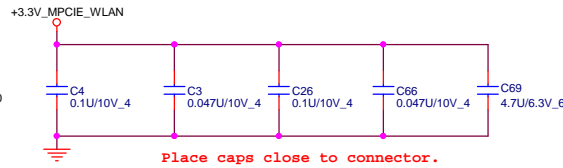
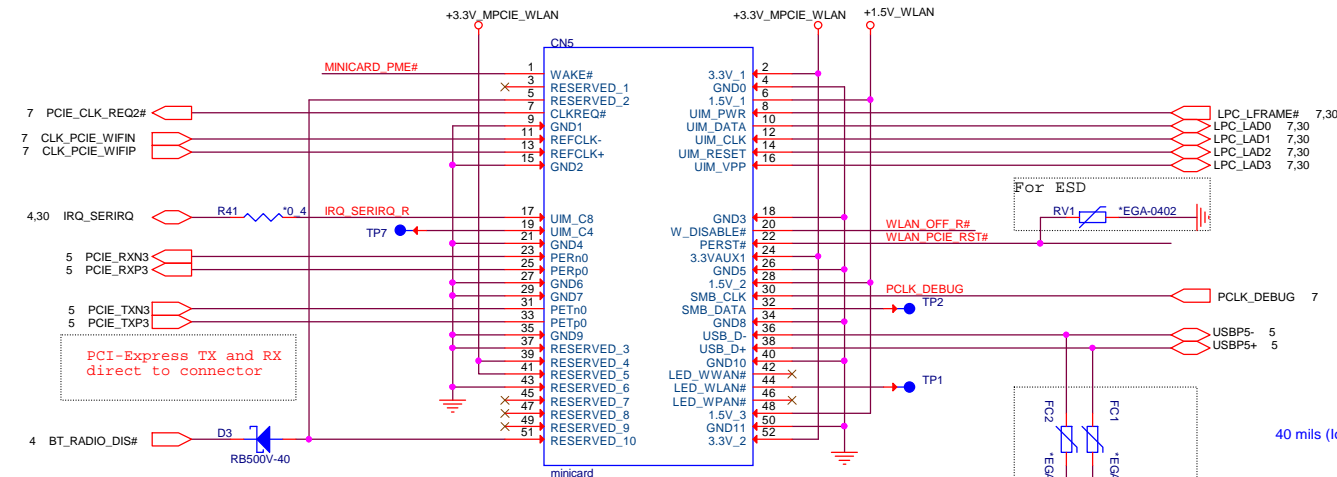
www.aitech1.ru

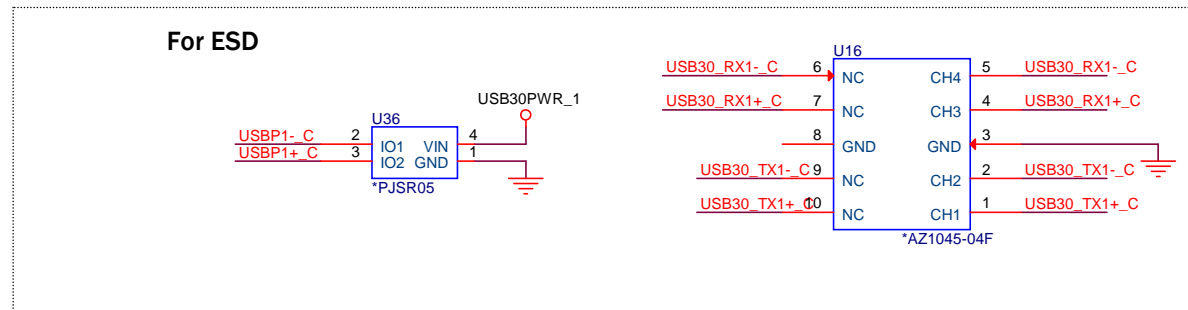
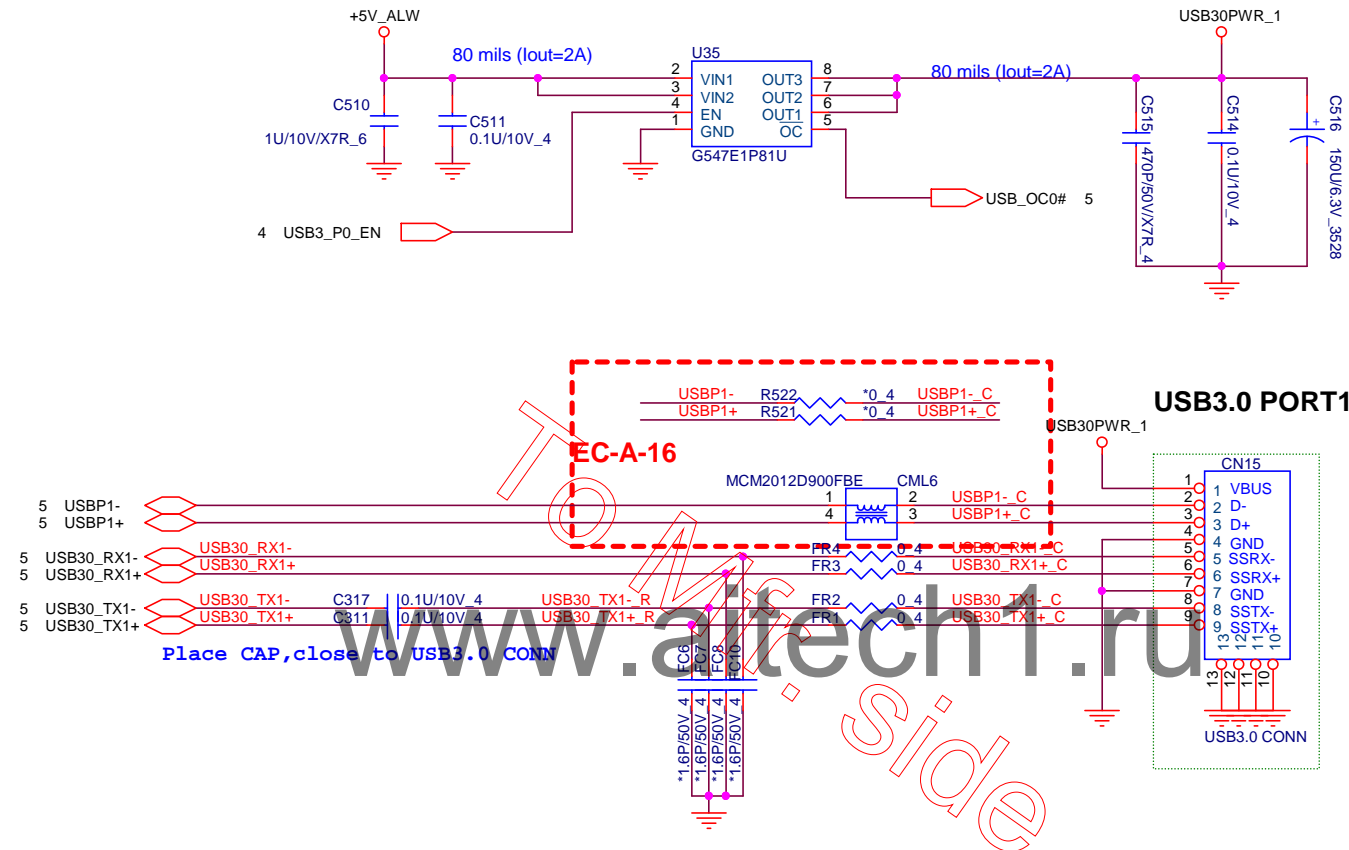
		PROJECT : ST6A	
		Quanta Computer Inc.	
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Mini PCIE Wifi/BT connector

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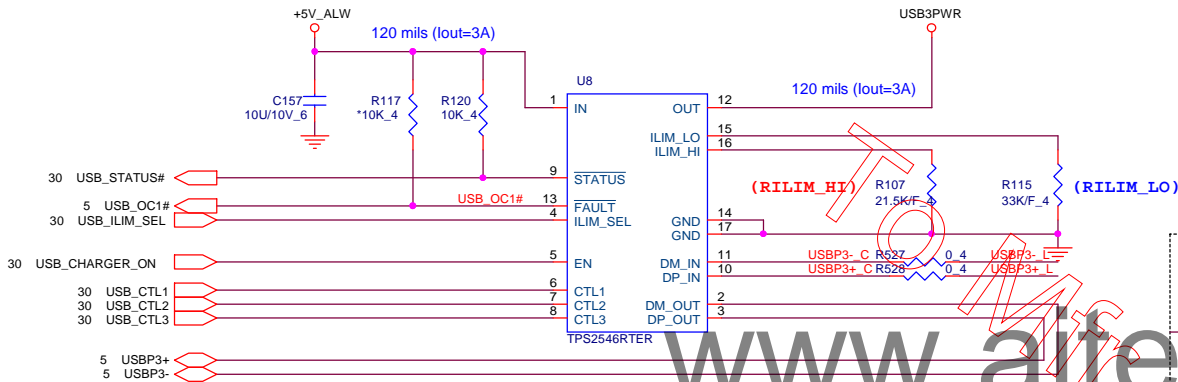
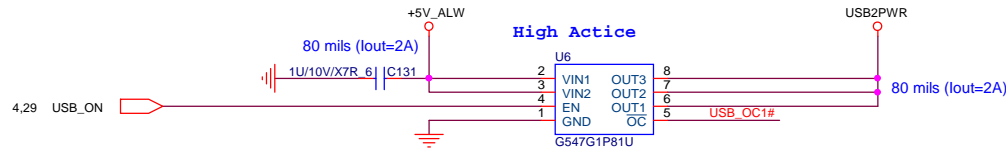




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	USB3.0 x1	1A
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USB 2.0 Port *2



RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:

1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used

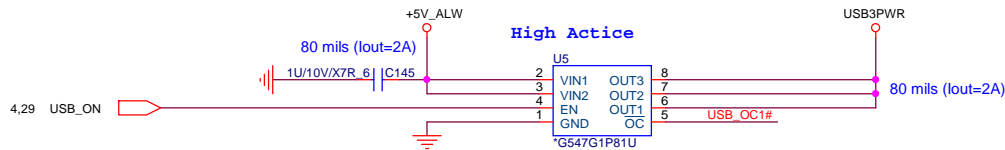
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.

The following equation programs the typical current limit:

(1)

RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$I_{OS_typ}(mA) = \frac{50,500}{(R_{ILIM_XX}(k\Omega) + 0.1)}$$



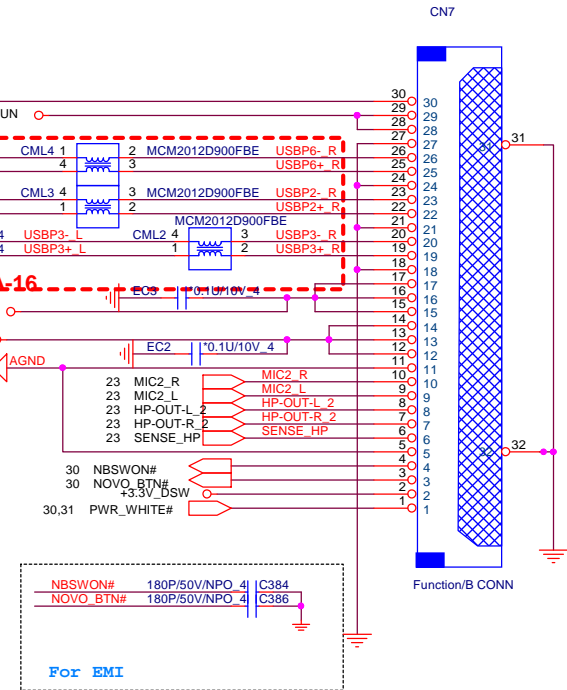
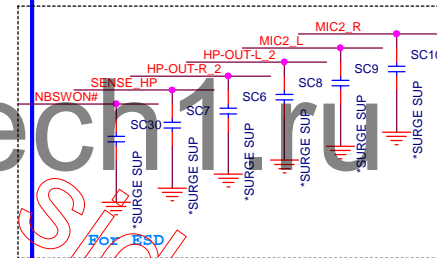
12,14,28,35,36,37,38,39,41,42,43,44 +5V_ALW
4,6,8,12,23,24,27,31,35,36,41,44 +3.3V_DSW
2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,30,31,32,34,35,40,41,42 +3.3V_RUN

29

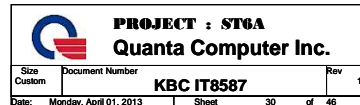
Card reader

USB2.0 Port 2

USB2.0 Port 3



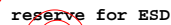
EC-A-04



14'' KB



Invensense total solution board



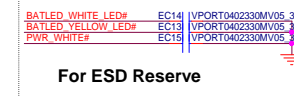
Volume/B




+3.3V_RUN

31

LED /B

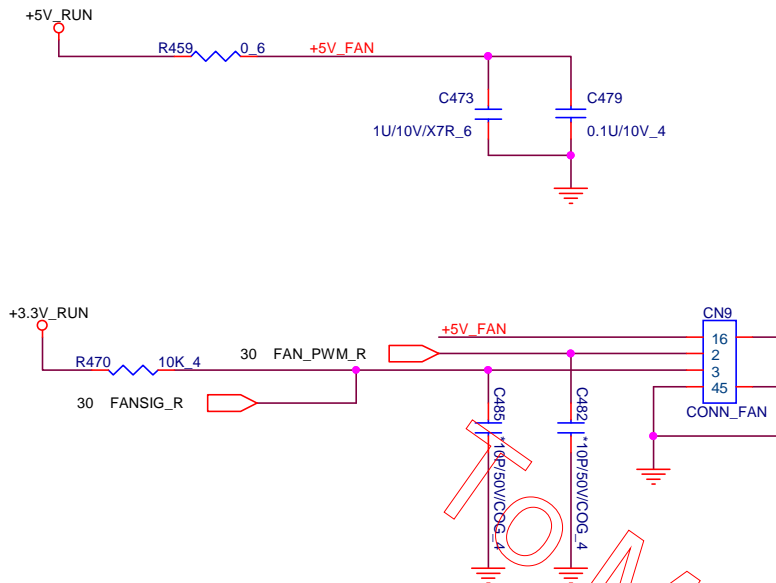


 PROJECT : ST6A Quanta Computer Inc.			
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KB/TP/LID			
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FAN CONTROL

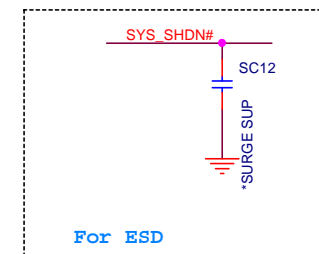
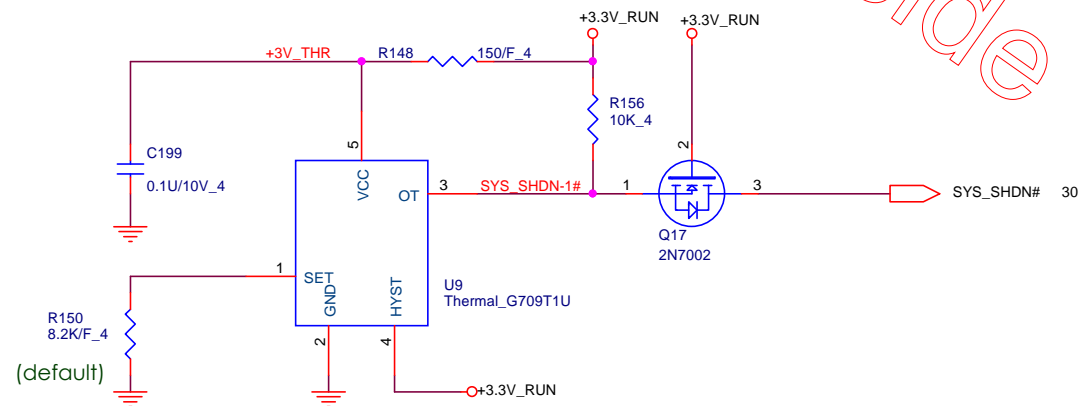
2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,34,35,40,41,42 +3.3V_RUN
22,23,25,35,40,41,42 +5V_RUN

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Thermal Sensor



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A

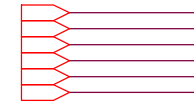
B

C

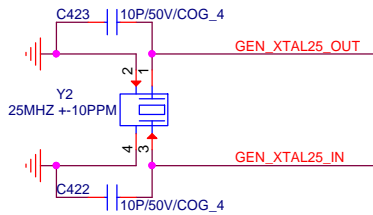
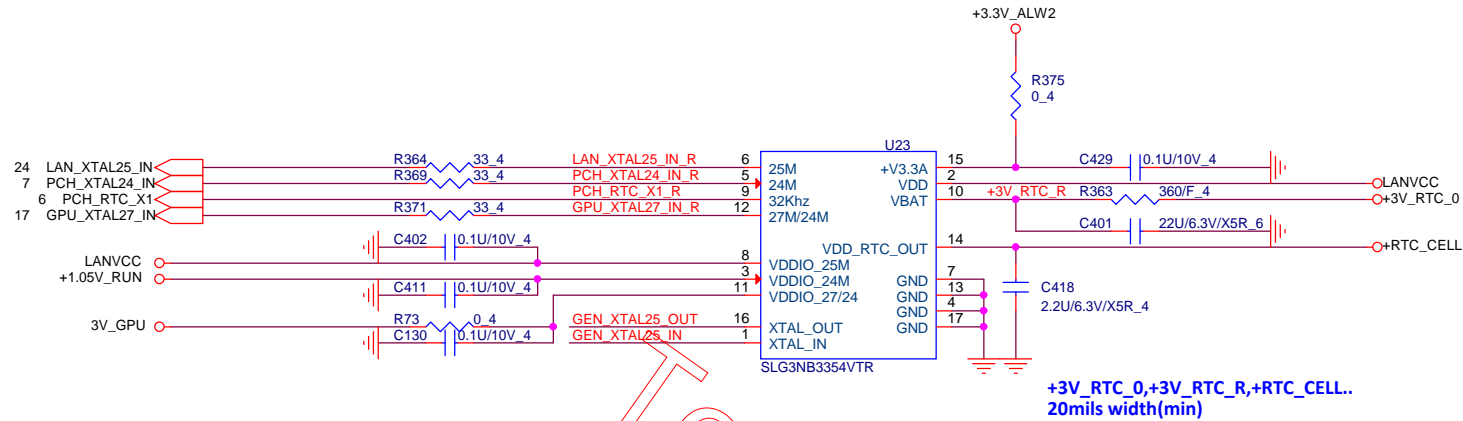
D

E

6,21,23,30,31,35,36 +3.3V_ALW2
24,42 LANVCC
6 +3V_RTC_0
6,12,30 +RTC_CELL
6,9,12,34,38,40,42,44 +1.05V_RUN
15,18,34,43,44,45 3V_GPU



33



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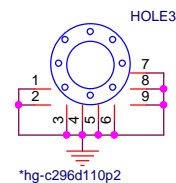
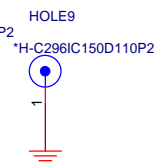
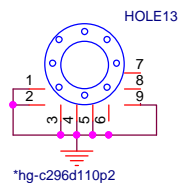
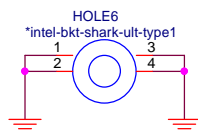
SLG3NB3354VTR(AL003354001)====>DIS
32Kx1+24M*1+25Mx1+27Mx1
1.S430-DIS --> SLG3NB3354
2.S430-UMA --> SLG3NB3355



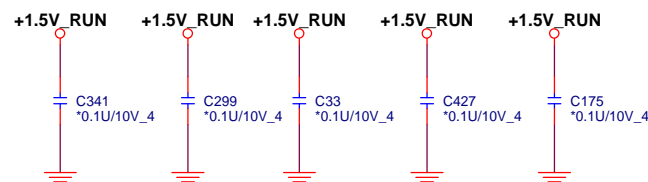
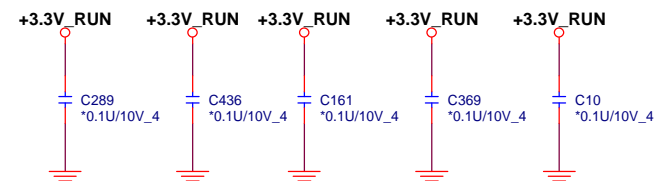
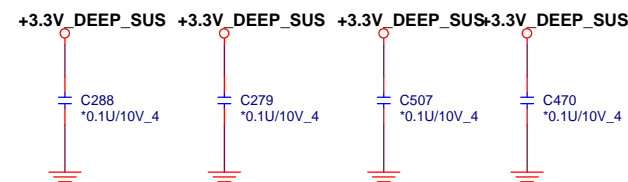
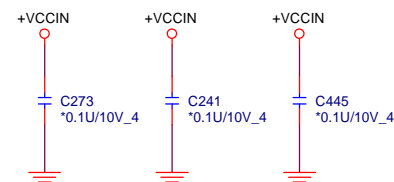
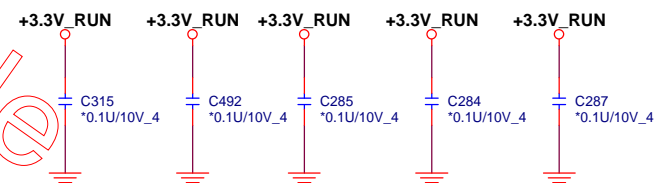
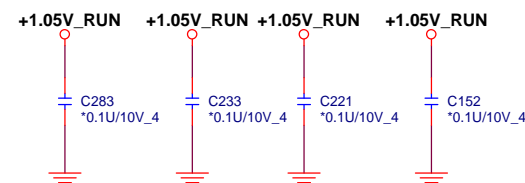
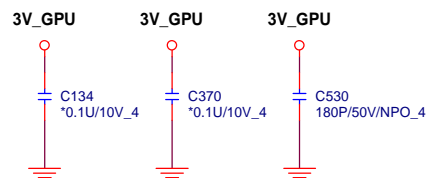
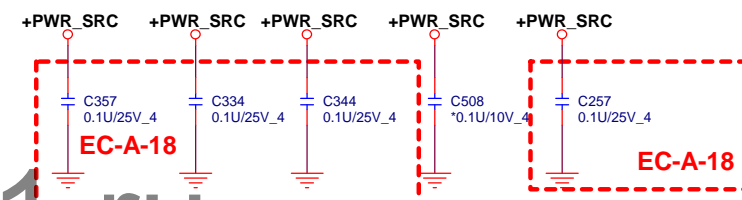
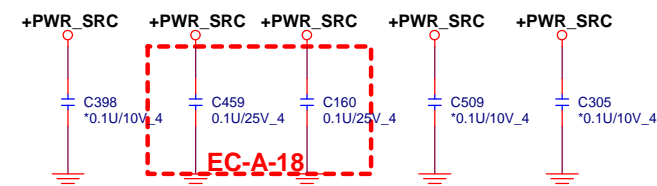
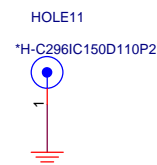
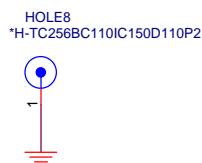
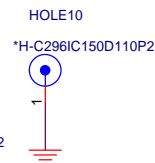
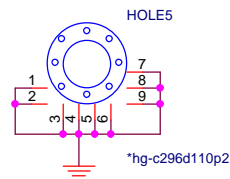
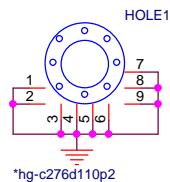
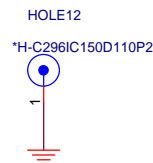
PROJECT : ST6A
Quanta Computer Inc.

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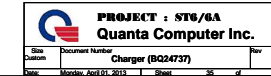
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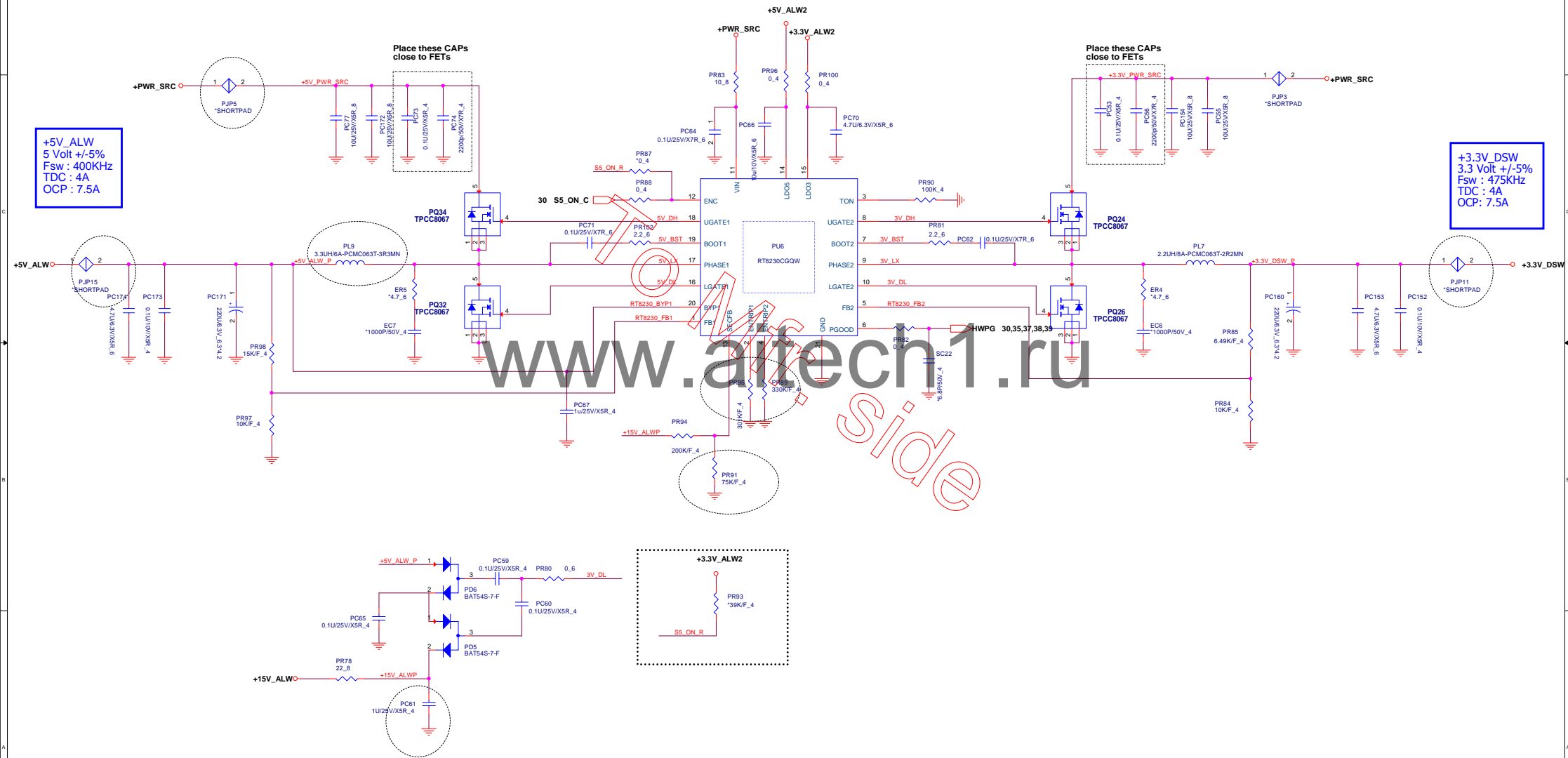


EC-A-18

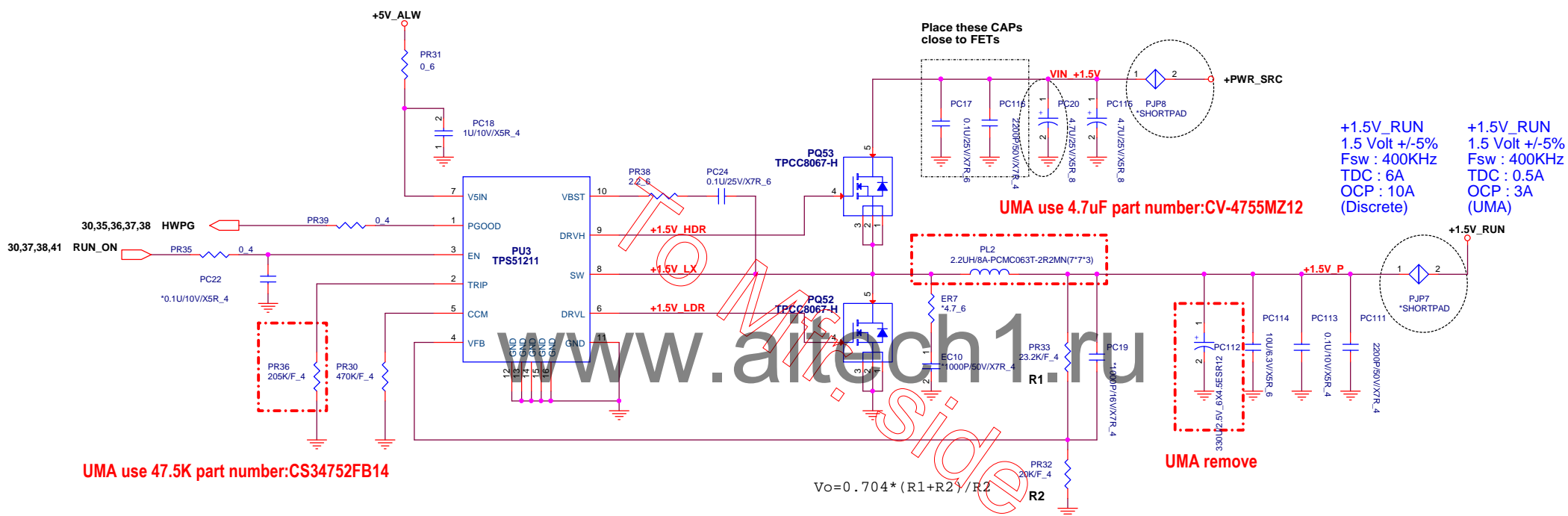


EMI reserve







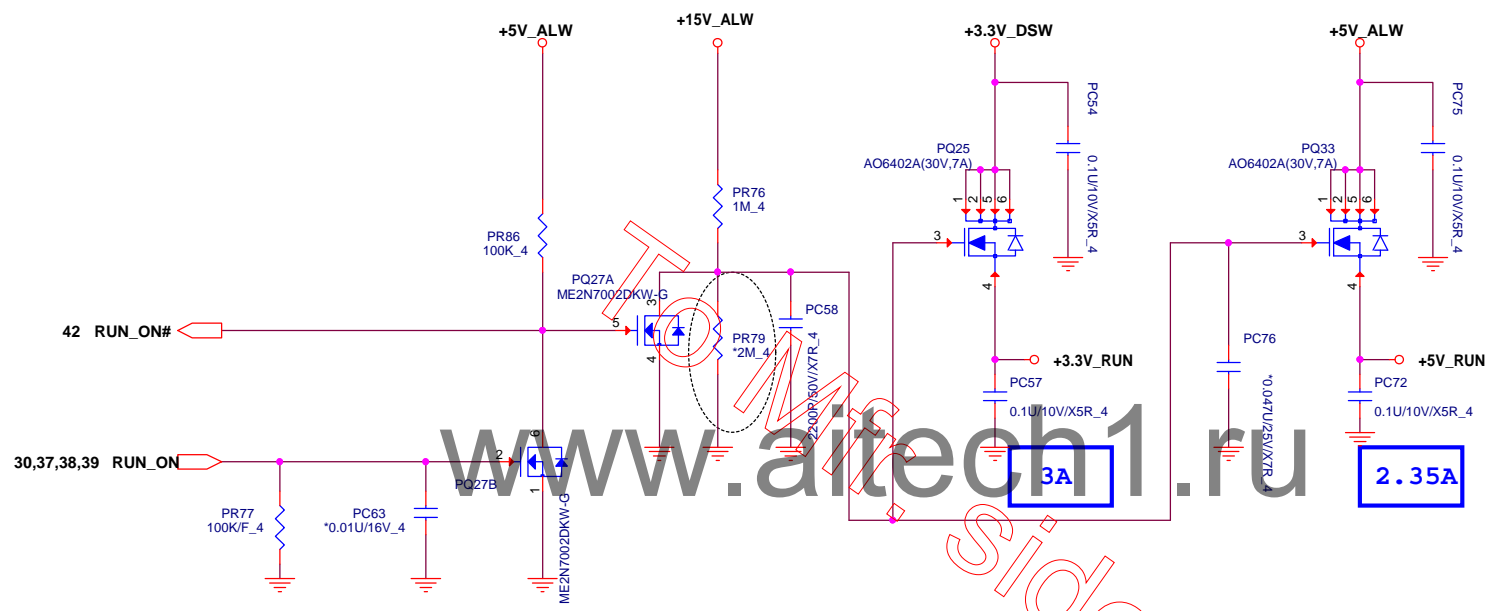




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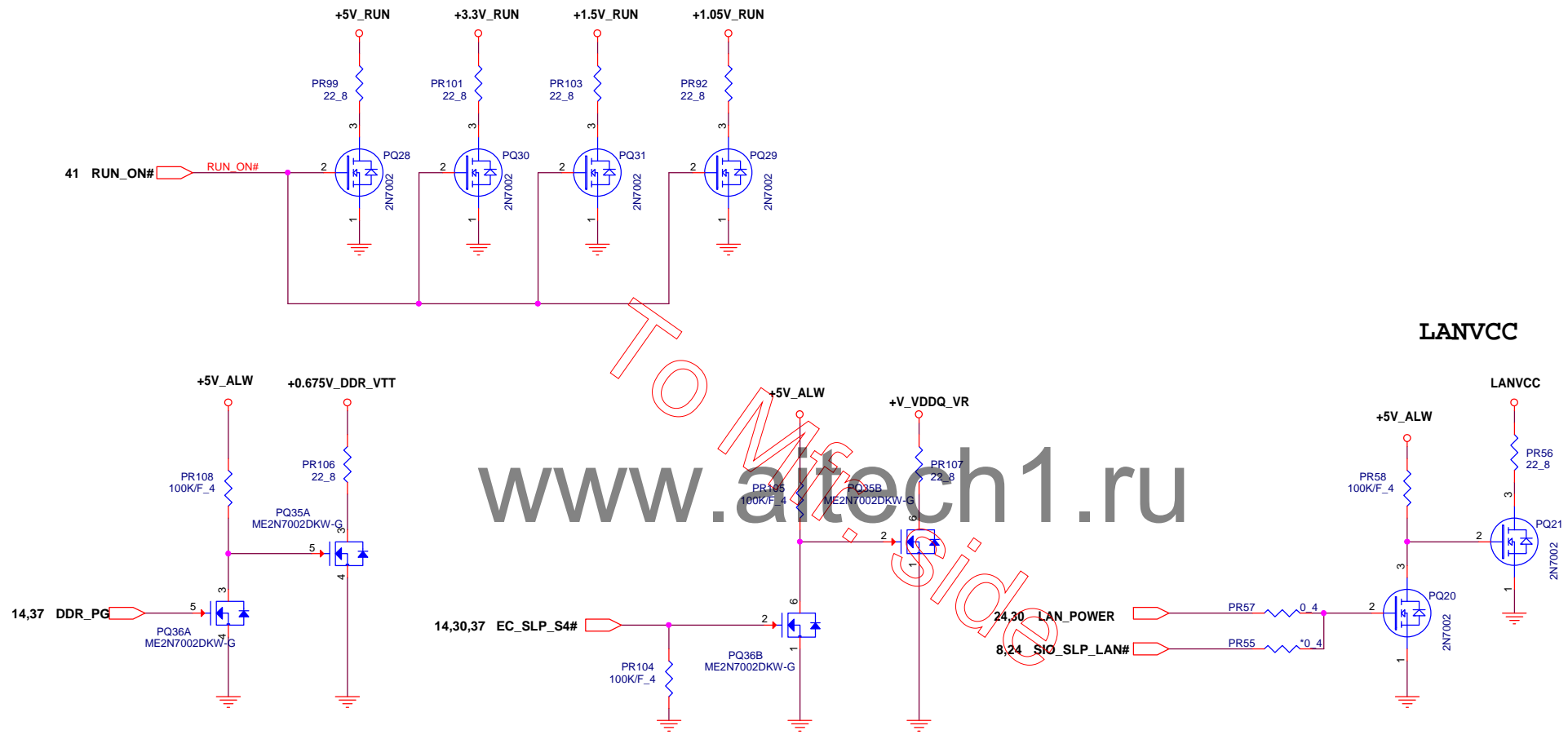
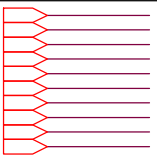
12,14,28,29,35,36,37,38,39,42,43,44
 2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,42
 4,6,8,12,23,24,27,29,31,35,36,44
 6,9,12,33,34,38,40,42,44

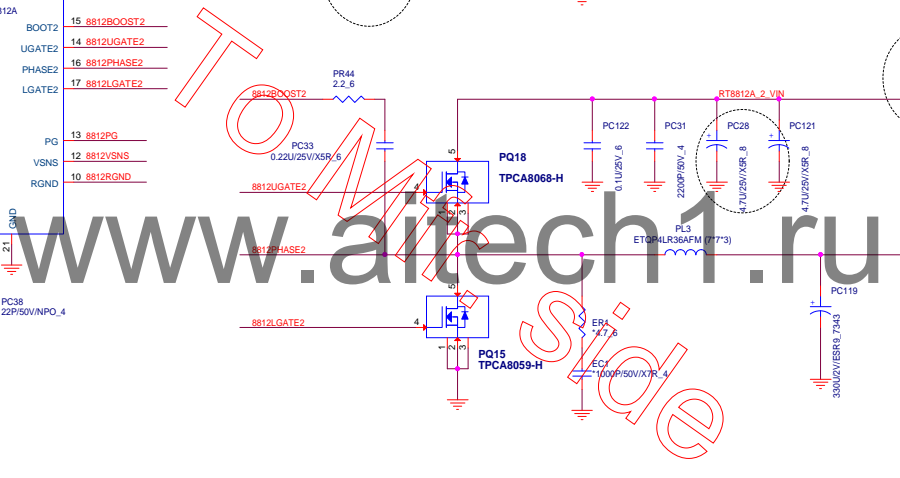
+5V_ALW
 +15V_ALW
 +5V_RUN
 +3.3V_RUN
 +3.3V_DSW
 +1.05V_RUN

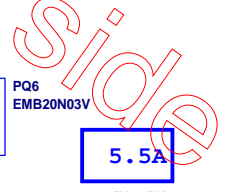


DISCHARGE

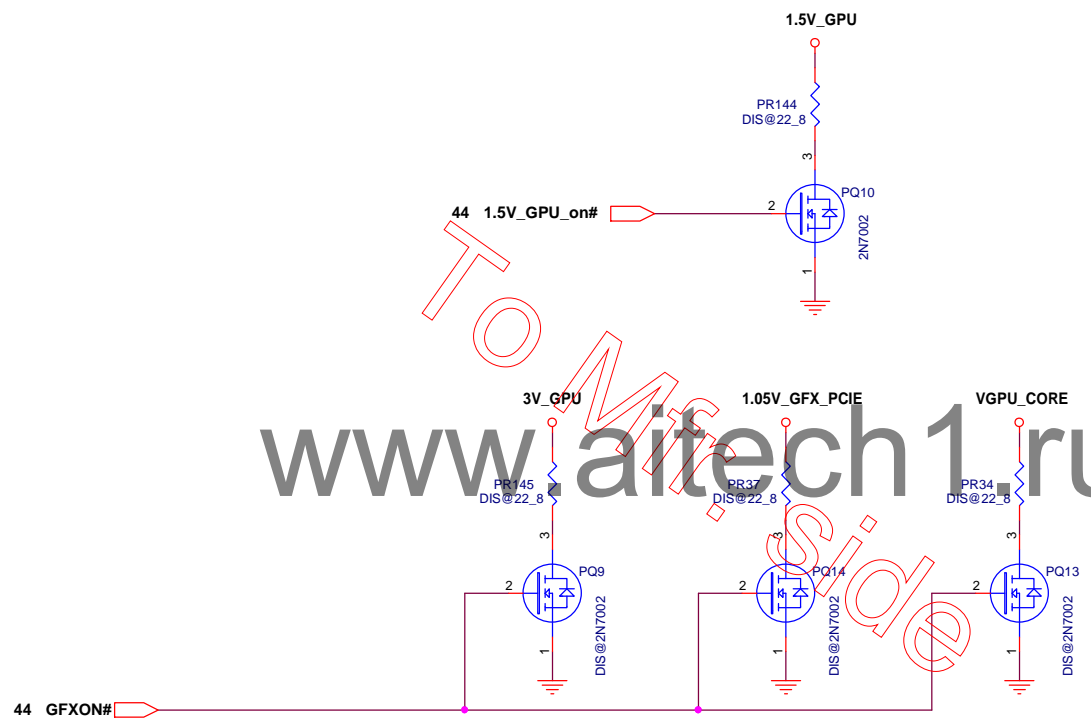
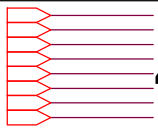
12,14,28,29,35,36,37,38,39,41,43,44	+5V_ALW
22,23,25,32,35,40,41	+5V_RUN
2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41	+3.3V_RUN
12,23,27,34,39,44	+1.5V_RUN
6,9,12,33,34,38,40,44	+1.05V_RUN
14,37	+0.675V_DDR_VTT
4,5,6,7,8,12,14,34	+3.3V_DEEP_SUS
9,14,37	+V_VDDQ_VR
24,33	LANVCC
36,41,44	+15V_ALW







12,14,28,29,35,36,37,38,39,41,42,43,44 +5V_ALW
2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41,42 +3.3V_RUN
12,23,27,34,39,42,44 +1.5V_RUN
6,9,12,33,34,38,40,42,44 +1.05V_RUN
14,37,42 +0.675V_DDR_VTT
9,14,37,42 +V_VDDQ_VR
24,33,42 LANVCC
36,41,44 +15V_ALW



SDV~SIV

2013

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-A-01	21	02/07		Change touch panel VCC control to +3.3V_RUN and stuff R17
EC-A-02	21	02/07		Add +3.3V_RUN to provide LCD panel EDID VCC and stuff R22
EC-A-03	20	02/08	C147	depop C147 from vendor request
EC-A-04	29,31	02/22	U10,C466	remove U10,C466 for lid change to sensor B
EC-A-05	29,31	03/05		sensor hub remove and reserve light sensor for I2C interface
EC-A-06	29	03/05	R528,R528	add R527,R528 to avoid stub
EC-A-07	7	03/05		CLKREQ change
EC-A-08	24	03/05		lan surge solution change
EC-A-09	21	03/06		RTD2132R support initial PWM to product LCDVCC
EC-A-10	21	03/06	R502,R504,R506,R509 R510,R511,R512,R513	change value to meet design guide
EC-A-11	29	03/13	R107	change to 21.5K for charger limit setting
EC-A-12	15	03/15		Q10 pin2 change to GFXPG control
EC-A-13	20	03/11	U24	depop
EC-A-14	12	03/12		change to +5V_ALW
EC-A-15	21	03/12	CN4	Change to 10 pin conn.
EC-A-16	29	03/18	CML2,CML3,CML4,CML6 R85,R90,R96,R101,R118,R119,R521,R522	CML2,CML3,CML4,CML6 pop for EMI suggestion R85,R90,R96,R101,R118,R119,R521,R522 depop for EMI suggestion
EC-A-17	22	03/18	R264,R265,R266,R267	R264,R265,R266,R267 pop for EMI suggestion
EC-A-18	34	03/18	C160,C257,C334,C357 and C459	C160,C257,C334,C357 and C459 pop for EMI suggestion
EC-A-19	30	03/19		KB_LOCK_BTN# pull up to +3.3V_ALW2
EC-A-20	21	03/19	R20,R21,CML7	delete R20,R21 and add CML7
EC-A-21	21	03/22	U39,R535,C529	reserve to meet LCD off sequence



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Quanta Computer Inc.

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